cadence™

Application Note
Vertical Conductive Structure (VeCS)
Allegro PCB Editor

Allegro/OrCAD Product Engineering
Cadence Design Systems
Ed Hickey
Mike Catrambone

Table of Contents

Vertical Conductive Structure (VeCS)

As design complexity and density increases it sometimes requires the designer to leverage different via technologies to successfully route into larger pin count devices while maintaining the highest level of signal integrity. Using Thru Hole Vias can take up a lot of valuable board space, moving to smaller Blind Vias reduces the via size but will require larger Buried Vias to complete the connections deeper in the board. Another costly alternative is using Every Layer Interconnect (ELIC) technology with each layer pair having its own copper filled, laser drilled MicroVias. Stacking these MicroVias on top of each other between layer pairs can extend the connection between any two layers in the board. These via technologies may successfully route the design but could cause the layer count to raise and if not done correctly could lead to signal integrity issues.

There is a new technology that can reduces layer count and improves signal integrity without the need got sequential technologies, Vertical Conductive Structure (VeCS). VeCS is different than traditional Thru Via, MicroVia and ELIC designs which is more expensive as it requires a high number of lamination, drilling and plating cycles to build up a reasonable number of layers. Using VeCS combines routing channels for better utilization of the channel escaping out large pin count devices. The larger routing channels allow more routes to escape with a more reliable/solid plane reference without the swiss-cheese effect normally seen other via technologies. For more details about VeCS Technology please visit the NextGIn Technology website @ https://www.nextgin-tech.com/

In Allegro, VeCS Structures are nothing more than a mechanical symbol that can be free placed or placed inside of a BGA field to take advantage of this new routing escape technology. No major changes were required to support these new structures in Allegro PCB Designer except for a manufacturing output update to generate limited depth (blind) drill files for pins in support of VeCS-2 blind depth structures. Taking advantage of the 17.2 Padstack Editor which support by-layer keepouts as well as adjacent layer keepouts to ensure manufacturability when these structures are used in a layout. These structures are created as library objects, so they can be easily leveraged across many designs for commonly used device escapes. If a structure requires a change it can be made in one place with all instances refreshed in the layout.

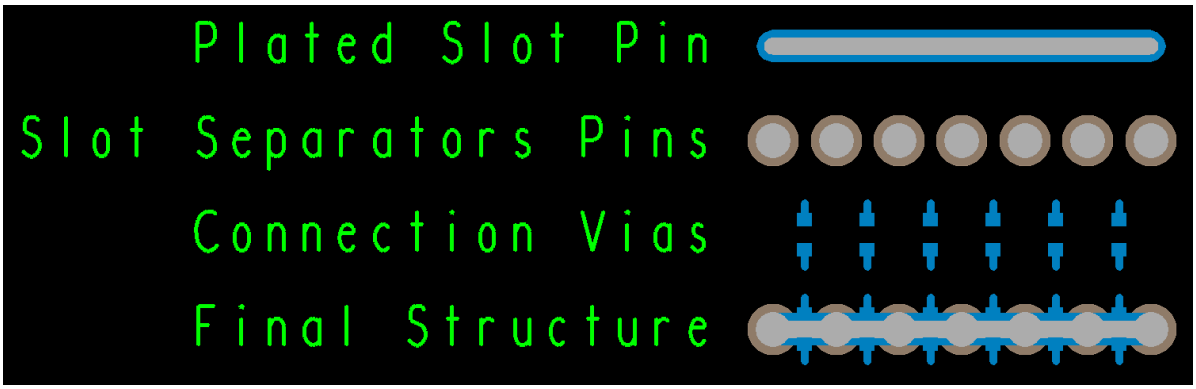
Definition of VeCS Structure

VeCS Structure Overview

VeCS Structures are built as mechanical symbols using Pins and Vias in the Allegro Symbol Editor. These mechanical symbols are then placed in the design as needed for routing, no need to add VeCS Structure symbols to the schematic. Standard VeCS Structures can utilize thru drill features (VeCS-1) but also be constructed using blind drill features (VeCS-2).

Below is a description of the different entities in a VeCS Structure:

- Plated Slot defined as Pins
  - Pins without logic pin number assignment
- Non-Plated slot separators defined as Pins
  - Slotted hole could be used for finer pitch BGA pin fields
- Connection Vias defined as a Via with stub traces
  - Vias adopts BGA pin net once stub trace end-point contacts the BGA pin center
  - To expedite creation, the Connection Via/Cline stub arrangement could be created in the layout then imported into the Symbol Editor using a Sub-Drawing
- Arrange the different objects to form the final VeCS Structure



- **Note**: The Pad and Drill sizes used for the Pins/Vias are driven by its application in the design. (i.e. BGA Pitch and Ball Pad sizes)
  - For latest VeCS Design Rules and Application notes for different packages visit the NextGIn Technology web site (http://www.nextgin-tech.com)

Padstack Generation – 1 mm BGA / 0.045 mm Ball Pads

Plated Slots

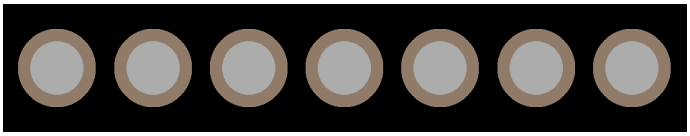
- Plated slot used as a base for the structure which does not directly connect to a net
- Drill = **5.254 mm x 0.254 mm**
    - X Size slot = Span of BGA Pads connection + Y Size slot
- Regular Pad (All Layers) / Mask Pad (External Layers) = **Oblong 5.508 mm x 0.508mm**
- Anti Pad = **Oblong 5.127 mm x 0.127 mm**
    - Anti Pad is smaller than Drill to allow Connection Via attachment to slot hole wall on negative planes
    - Anti Pad on Connection Via and Keepout in Non-Plated Hole will isolate non-connected locations
- Thermal Pad (All Layers) = **None**
    - Plated Slot is not directly connected to a net, no thermal required
- Adjacent Layer Keepout = **Oblong 5.508 mm x 0.508 mm**
    - Mechanical drill overshoot clearance for VeCS-2 (Blind depth)
- Plated Slot Placement
    - Orthogonally placed between BGA Ball Pads

Plated Slot

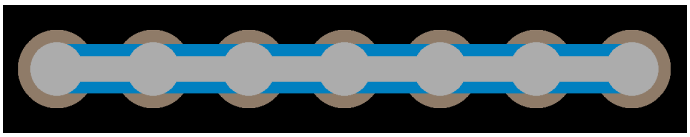
Alignment in BGA Pin Field

Non-Plated Hole/Slot (Slot separator)

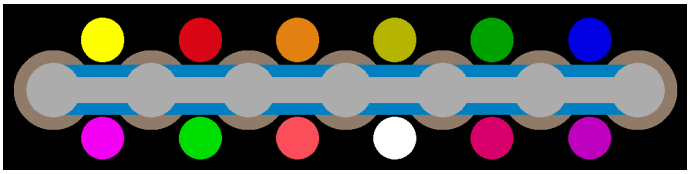
- Non-Plated hole is used to divide the slot into multiple sections so individual connections can be made by traveling down the slot hole wall.
- Drill = **0.559 mm**
- Regular Pad (All Layers) = **Circle 0.127 mm**
- Anti Pad / Thermal Pad (All Layers) = **None**
- Keep Out (All Layers) = **Circle 0.813 mm**
- Mask Pad (External Layers) = **Circle 0.356 mm**
- Adjacent Layer Keepout = **Circle 0.813 mm**
    - Mechanical drill overshoot clearance for VeCS-2 (Blind depth)
- Non-Plated Hole Placement
    - Spaced on 1 mm centers orthogonally placed between BGA Ball Pads aligned with Plated Slot



Non Plated Hole (Slot separator)



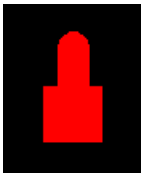
Plated Slot and Non Plated Hole (Slot separator) alignment



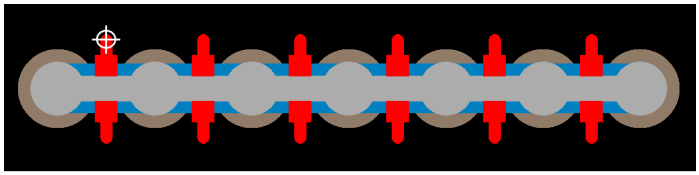
Alignment in BGA Pin Field

Connection Vias

- Connection Via adopts the BGA Pad net name using the Cline stub.
  - Cline width = **0.127 mm – 0.222 mm** (outward)
  - Cline length = **0.162 mm** (outward)
  - Cline stub is only required on the BGA Pad layer
- Drill = **None**
- Regular Pad (All Layers) = **Rectangle 0.228 mm x 0.222 mm**
  - Offset Y = **0.100 mm**
- Thermal Pad (All Layers) = **Circle 0.012 mm**
- Anti Pad (All Layers) = **Rectangle 1.000 mm x 0.350 mm**
  - Offset Y = **0.164 mm**
- Mask Pad (All Layers) = **None**
- Connection Via Placement
  - Offset from Plated Slot = **0.338 mm**
    - Edge aligned to the Plated Slot hole wall
  - Centered between Non-Plated Holes (Slot separators)

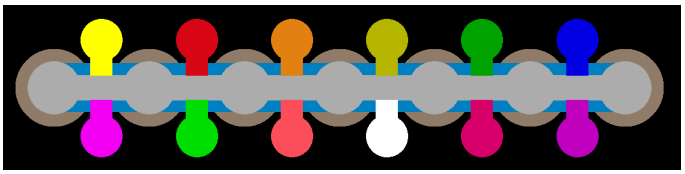


Connection Via with Cline stub



Plated Slot, Non Plated Hole (Slot separator) and Connection Vias alignment

Symbol orign @ Cline endpoint



Mechanical Symbol placed in the design, BGA Pin drive Connection Via net name

Finalize Mechanical Symbol

Properties assigned in the Mechanical Symbol

- Using ***Edit > Property*** and the **Find Filter** to enable objects for selection add the properties as outlined below:

  Pin Properties on the Plated Slot and Non-Plated slot separators:

  - **NO_SHAPE_CONNECT**
  - **ADJACENT_LAYER_KEEPOUT_ABOVE = 1 (VeCS-2 overshoot clearance)**
  - **ADJACENT_LAYER_KEEPOUT_BELOW = 1 (VeCS-2 overshoot clearance)**

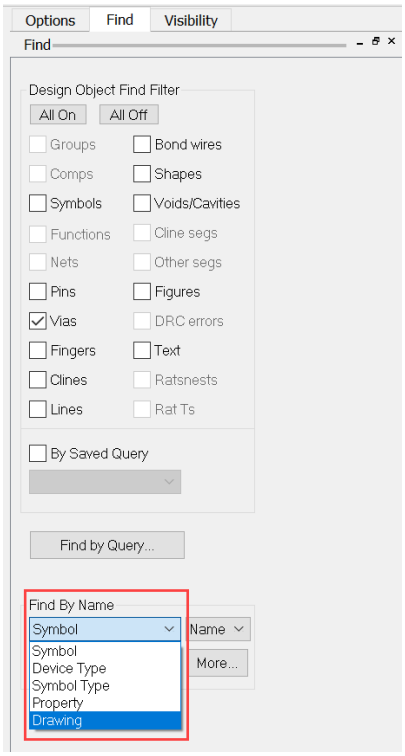
  Via Properties added on the Connection Vias:

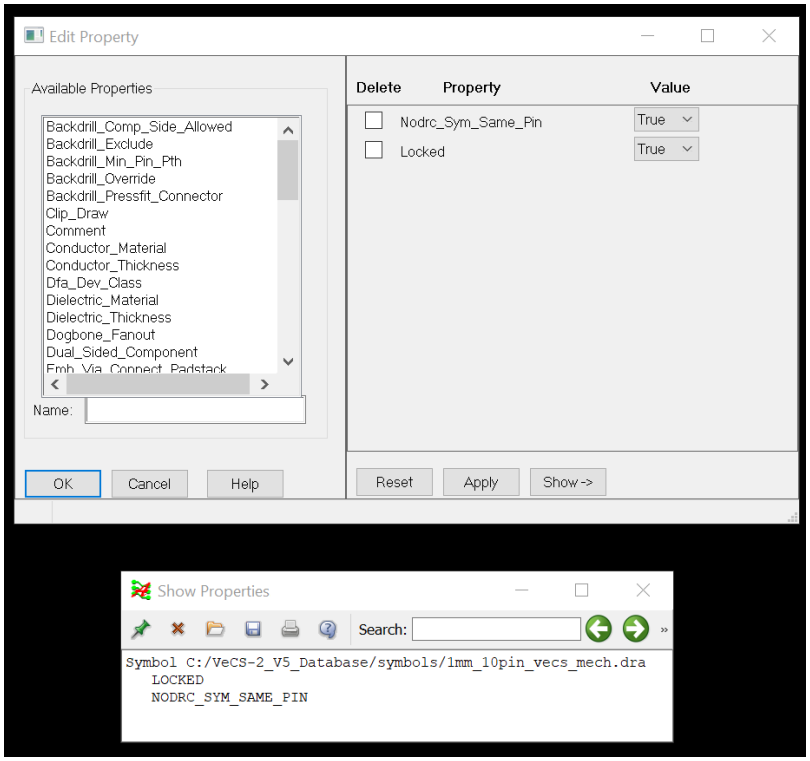
  - **DYN_MIN_THERMAL_CONNS = 1**
  - **DYN_THERMAL_CON_TYPE = ORTHOGONAL**

- Using ***Edit > Property*** and the **Find Filter** to select **Drawing** from the **Find By Name** pulldown to add the properties as outlined below:

  Symbol Drawing Level Property associated to the mechanical Symbol:

  - **LOCKED**
  - **NODRC_SYM_SAME_PIN**

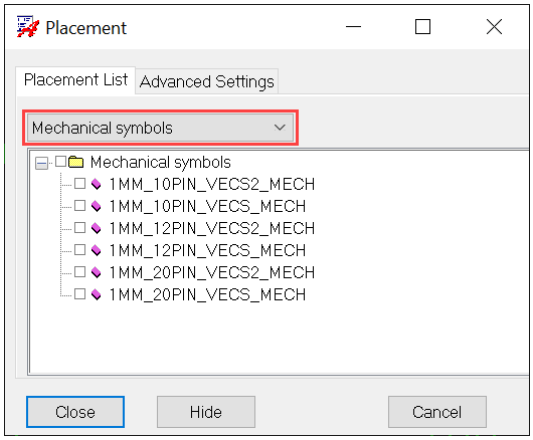




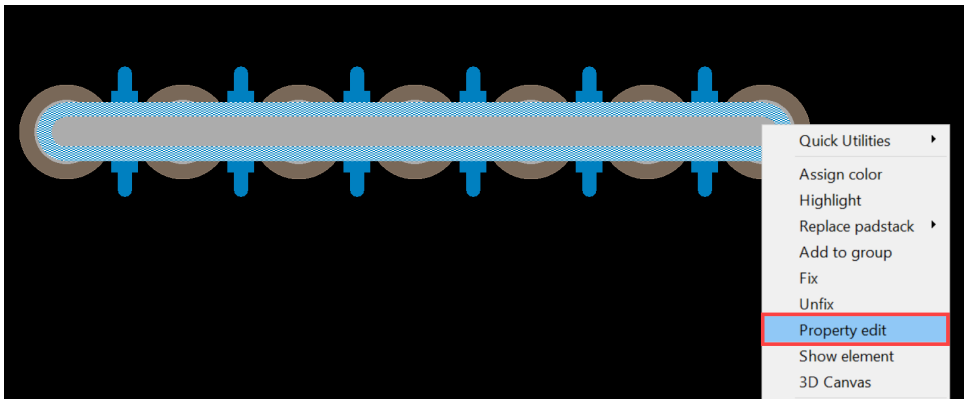
Using VeCS Structure

Placing in Layout

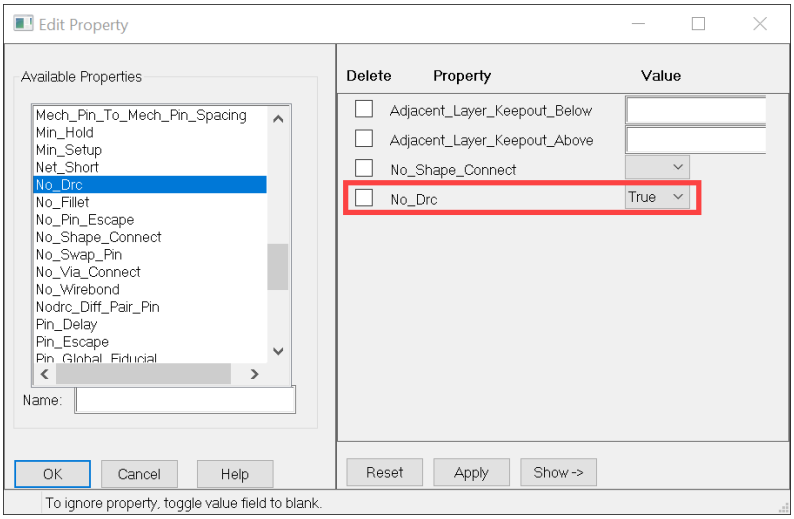
- Using ***Place > Manually*** select Mechanical Symbols for the filter pulldown and place the symbol in free space in the layout



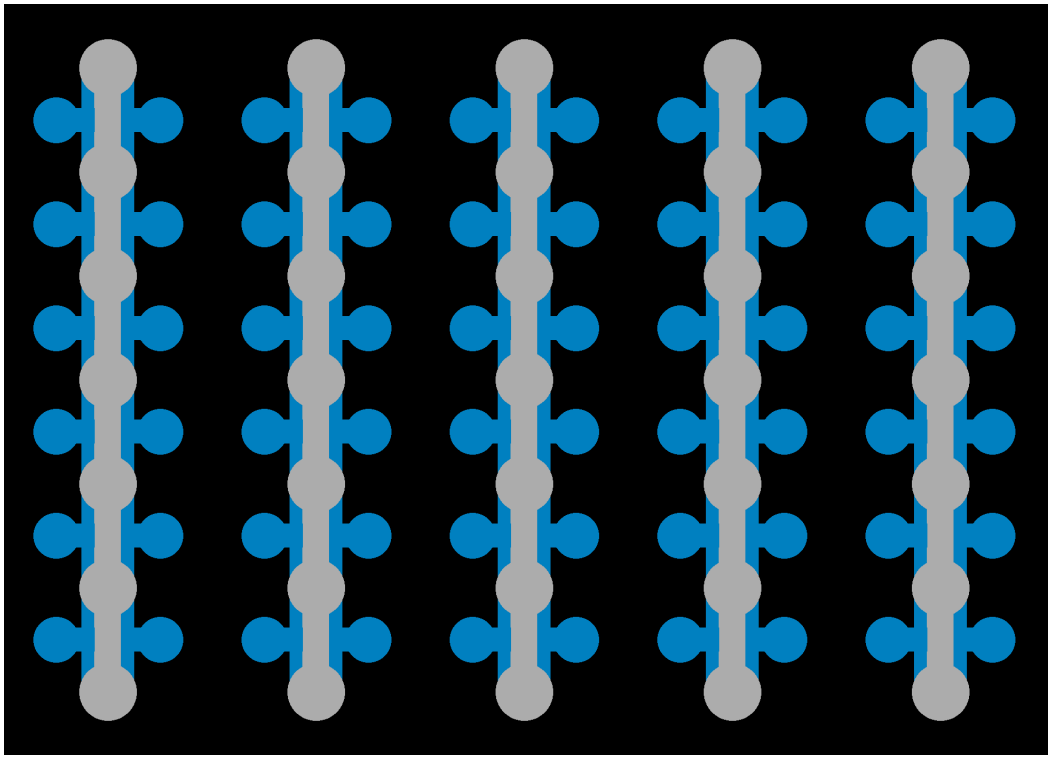
- Enable **Pins** in the **Find Filter**, window select all the pins on the placed VeCS Structure and ***RMB > Property Edit***



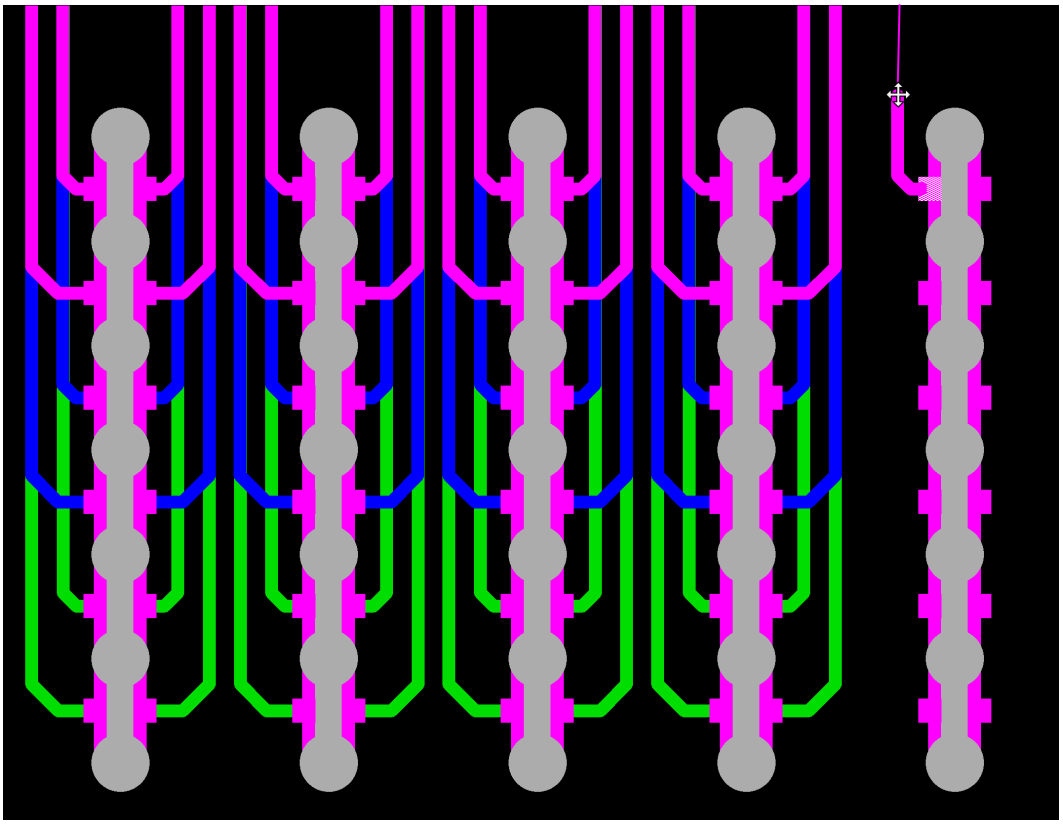
- Add the **NO_DRC** Property to the Pins



- Now freely copy the VeCS Structure inside of the BGA pin field, as required



- Turn on the inner layers and route to Vias along the slot walls using ***Route > Connect***



Changing Layer Depth (VeCS-2)

Using VeCS-2 Structures requires a change in the mechanical symbol and padstack to generate the appropriate blind drills when structures is placed in the layout.

- Cross Section in Symbol and Padstack must contain the Start/Stop subclass names to identify the blind depth of the VeCS-2 Structure.
    - It is not required to define the entire stack-up, just the Start/Stop subclass names must match the target design
- Padstack geometry definition on Start/Stop Layer drive the blind depth when placed in the design

Setting up Design Rules

Padstacks

With the advancements made in the 17.2 Padstack Editor there is no special design rules that are required to successfully use a VeCS Structure in the layout.

- **Plated Slots:** Adjacent Layer Keepout for mechanical drill overshoot clearance for VeCS-2
- **Non-Plated Hole/Slot (Slot separator)**: Keepout on All Layer for clearance to the Non-Plated hole or slot.
    - Utilizing by-layer keepouts and adjacent layer keepouts for VeCS-2 Structures

Pin Properties applied in the Layout

Placing the VeCS Structure in the layout will produce DRC Errors between the Plated Slot and the Non-Plated Hole/Slot (Slot separator) pins, which is expected. To eliminate these DRC Errors the designer must apply **NO_DRC** properties to the Pins of the VeCS Structure.

- This property can be added upon placing the first VeCS Structure and simple copy this structure to all the required locations in the design.

Fabrication Output

VeCS Structures in Allegro PCB Designer should work directly out of the box except when moving to VeCS-2 Structures (blind depth). To support VeCS-2, a manufacturing output change was made to generate the appropriate drill files for Blind/Buried Drills and Slots.

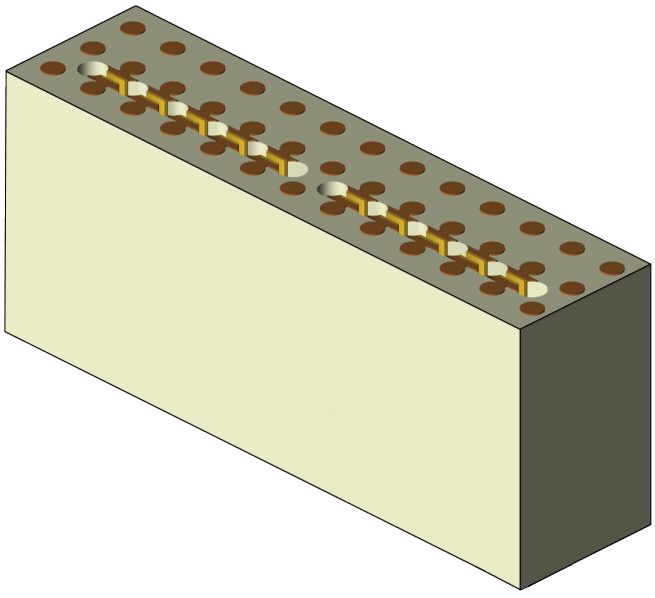
This manufacturing output change was made in 17.2 QIR5 (S031) – December 2017

DRILL CHART: TOP to LAYER_5

ALL UNITS ARE IN MILLIMETERS

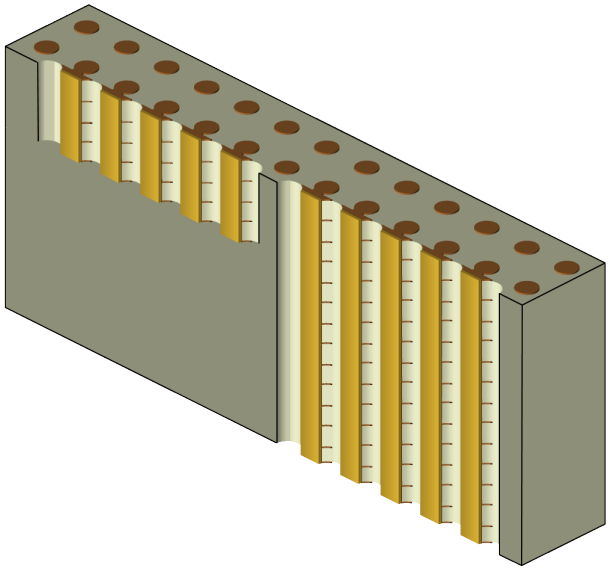
FIGURE	FINISHED_SIZE	ROTATION	TOLERANCE_DRILL	TOLERANCE_TRAVEL	PLATED	QTY
A	0.559	-	+0.076/-0.076	-	NON-PLATED	187
	5.254x0.254	90.000	+0.076/-0.076	+0.076/-0.076	PLATED	10
	5.254x0.254	0.000	+0.076/-0.076	+0.076/-0.076	PLATED	4
	6.254x0.254	0.000	+0.076/-0.076	+0.076/-0.076	PLATED	10
	10.254x0.254	0.000	+0.076/-0.076	+0.076/-0.076	PLATED	3

3D Canvas Display



3D Canvas View

Non-Plated Slot Separators divide the Plated Slot



3D Canvas Cut Plane View

Segmented Plated Slot Hole Wall connected on all Layers

VeCS-1 (Thru Depth)

VeCS-2 (Blind Depth)