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Connection to the Next Level

Application note

Fan-out Xilinx FLGA 2892 using VeCS.

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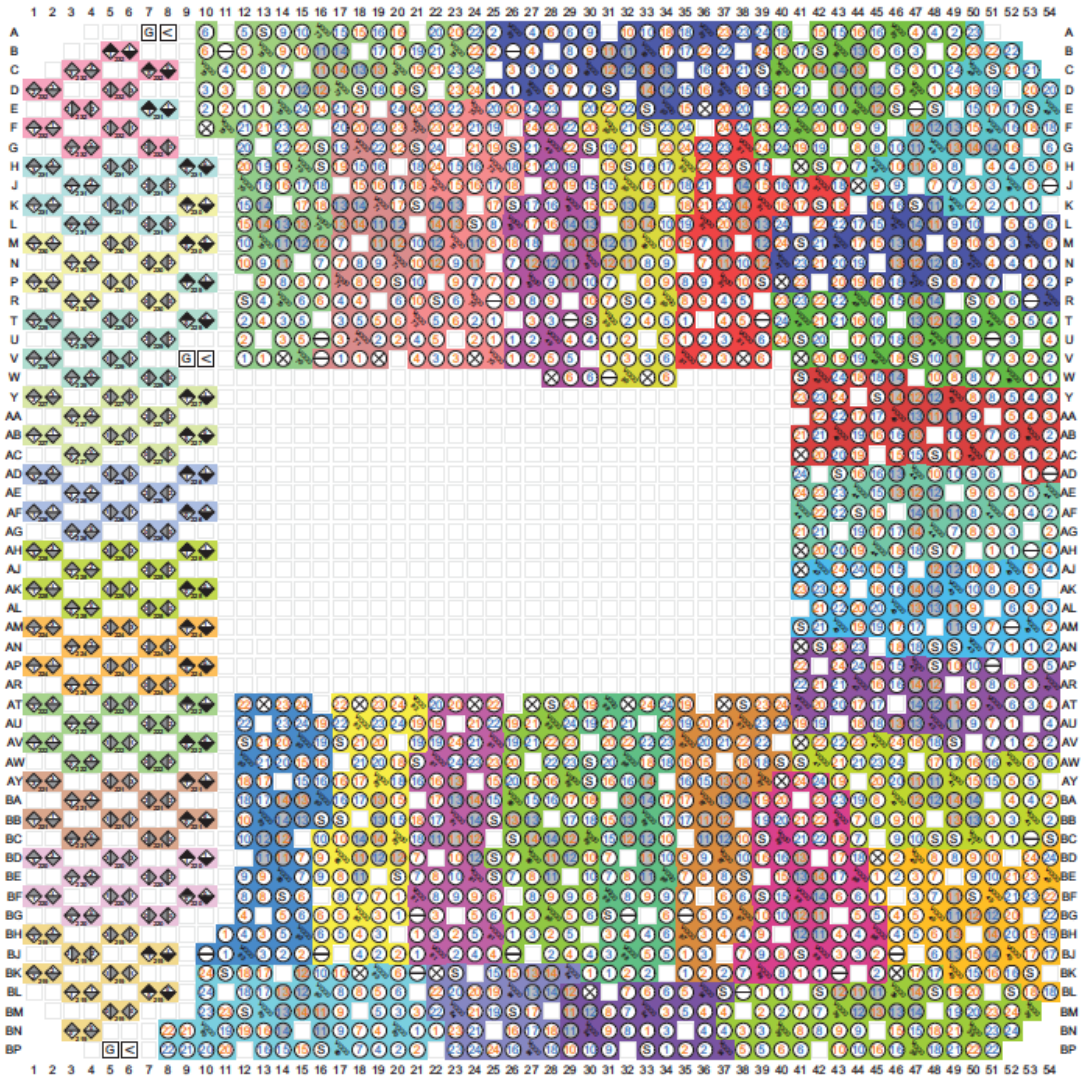
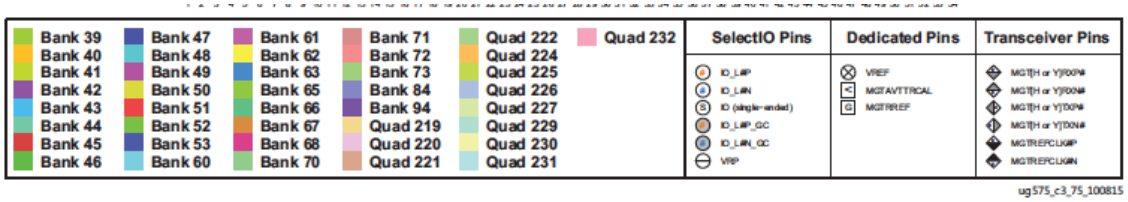
The objective of this document is showing the use of VeCS technology to fan-out from the Xilinx 2892 chip using the following constrains:

- Differential pairs with a minimum track width of 0,1mm the Banks and
- Differential high speed SERDES with a minimum trackwidth of 0,15mm (in order to minimise DC loss).
- All differential line to use reduced stub configuration.

Eventually we will conclude with the number of signal layers required for this fan-out and number of reference and voltage layers resulting in a complete stack-up. We will compare this with the conventional through hole technology. In this document we will not addressing process technology for the fabrication of VeCS.

The Xilinx chip is packaged in a 1.0mm traditional BGA consisting out of a pin count as shown below. The white boxes in between the coloured ones are the supply voltages and ground reference.
On the left had side an array of high-speed SERDES pairs is situated. The rest of the pins are banks with mainly differential pairs and control voltages.





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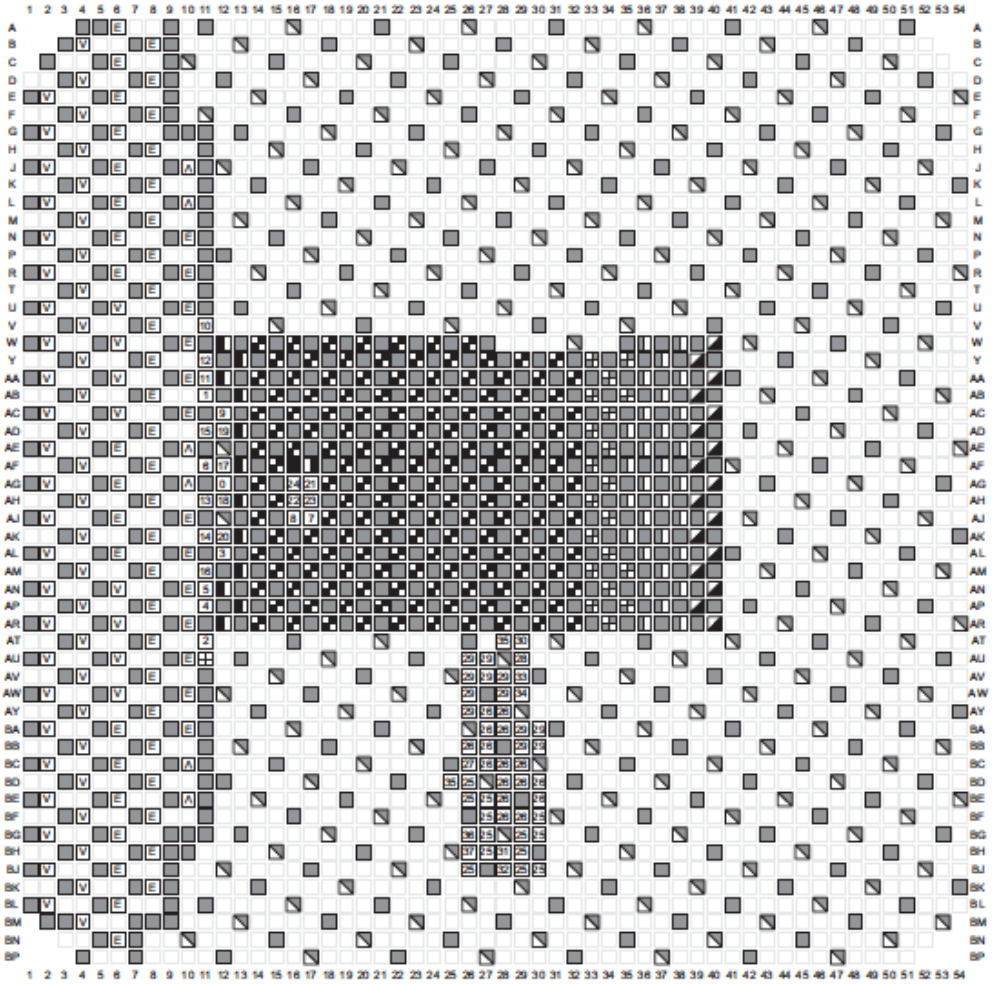
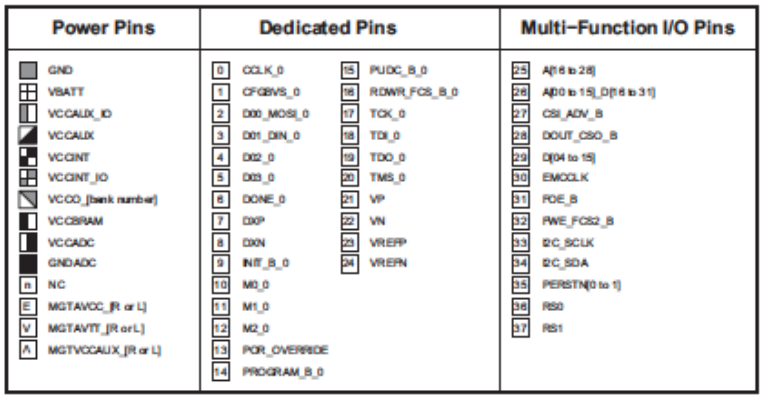
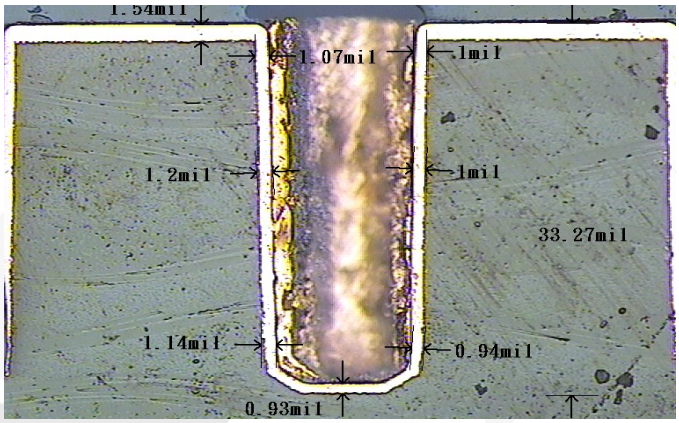
The Legenda to the pin assignment is given in the schematic above. The configuration on the GND pins is shown in the imgae below.



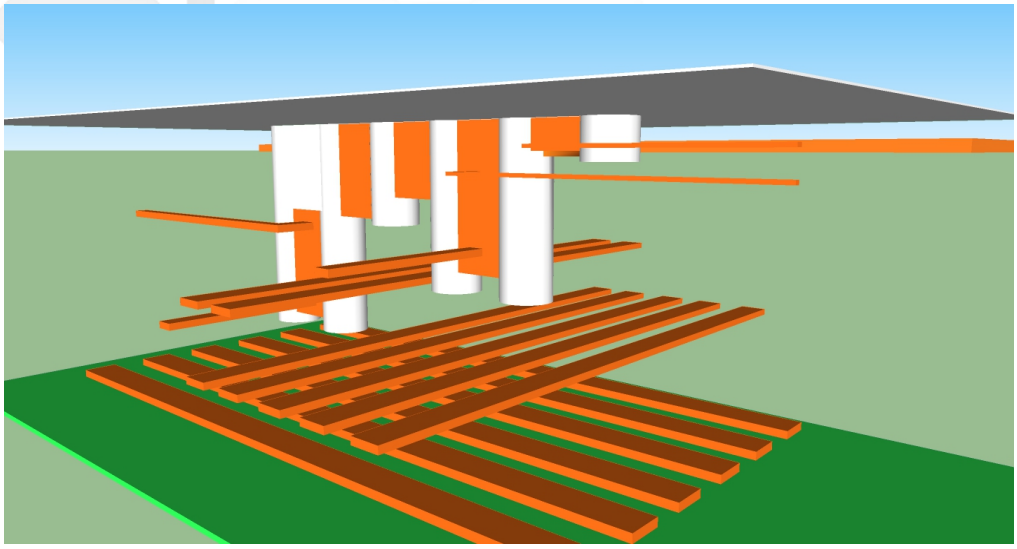


To achieve the goals in a as small as possible layer count we are going to use VeCS-2 technology. This is a blind / stub less slot technology that can go very deep into the board and basically connect to any layers. In a single slot we can combine it with through connections as shown in the next image.

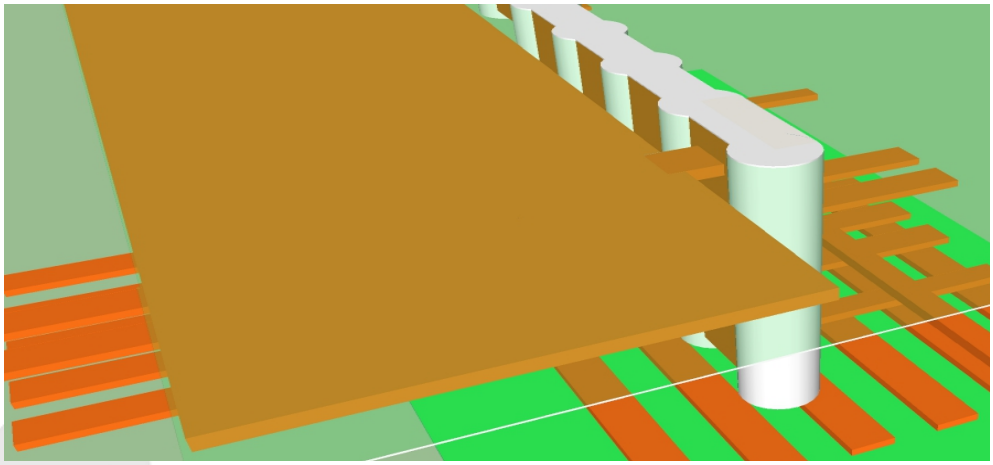
Following cross section is showing that plating deep slots is not a problem this in respect to blind hole technology that can only be plated to a maximum depth equal to it's diameter.



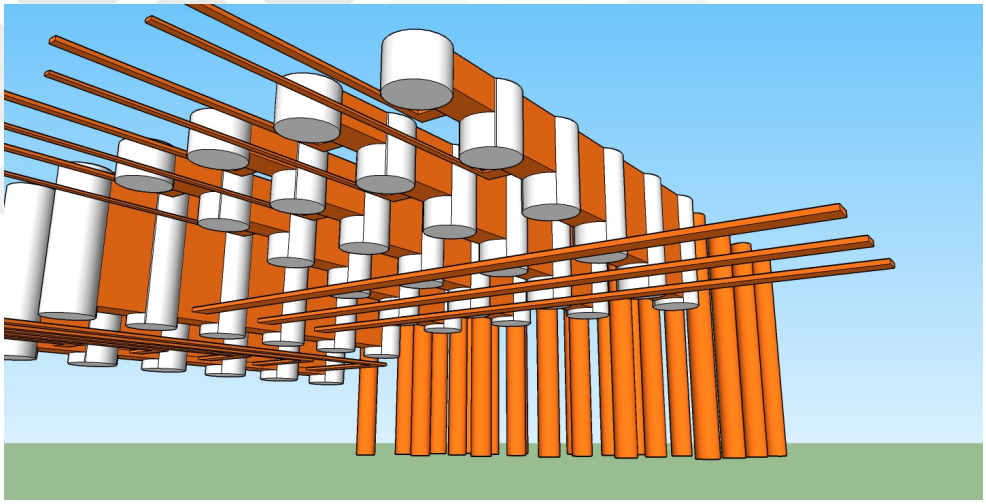
Following images show how VeCS is set-up. As you can see the advantage of only connecting to the layer you want to connect to is that the space below is free for routing and that the connection has a minimum stub-length. It is to the creator/designer how he or she wants to apply VeCS.



The ground and voltage planes are connected in the same way as shown in the next image.



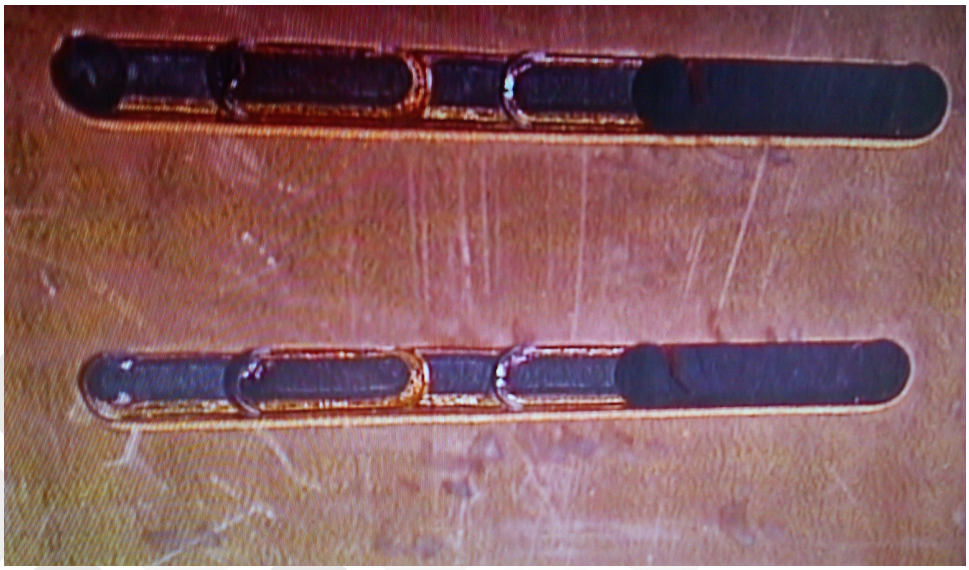
The following images show how we use VeCS-2 technology in a array construction. These images show also the advantage, not penetrating all layers creates huge amount of routing space. This is the same as Microvia/Anylayer technology with the difference that we do not need sequential lamination process for fabrication but use a single lamination cycle.



As shown in the image above as we go closer to the centre of the BGA we step further down into the board. We can even combine it with a section going al the way through the board. Many combinations are possible.

For the GND and supply voltage section in the centre of the board we use 0,3mm through hole we do not plan to route through this section. If required it can be done but the drill hole size need to be reduced from 0,3mm to 0,25mm.

A top view image of VeCS-2 slot is shown below seeing the different depth of copper plating. This picture is taken prior separation of the sections in order to see the differences. On the right hand side (darker section) the slot is going all the way through the board.

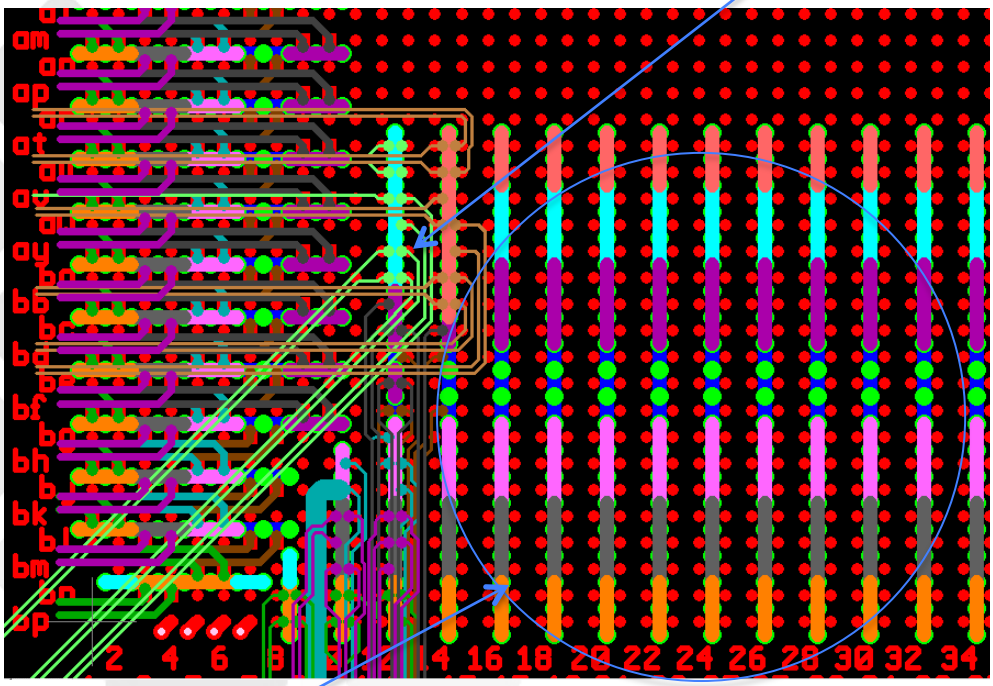


The technology for creating the VeCS-2 slot as used in this application is a 0,5mm slot. This wider slot gives us the ability to clean the bottom to split the slot in two parts creating 2 high-density connections. The width of the separation is 0,3mm.

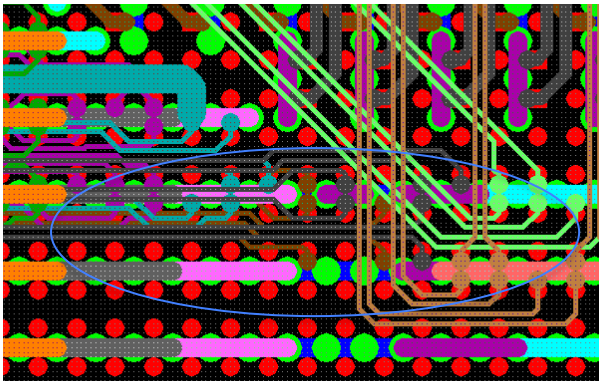
CAD design of the Xilinx 2892

With the design tool we were able to create the fan-out of the high speed SERDES section and we started with the fan-out of the banks as shown in the following images.

We are using VeCS-2 technology for the fan-out of the Xilinx chip giving us the ability to rout on all directions on the lower layers as there are less blockages as you step down in the board. This is shown on the green layer.

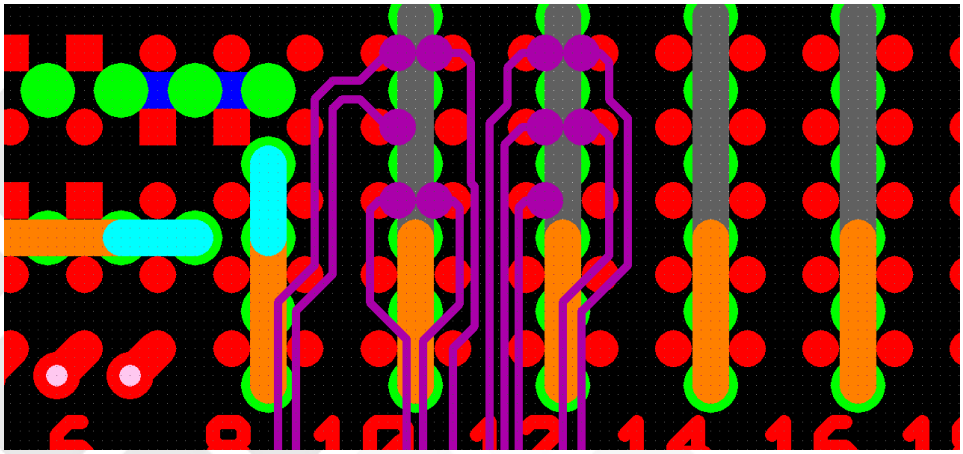


On the right hand side you see the slots represented in different depths. We have a total of 7 different depths for a total of 7 signal layers. As 7 layers would not be a good balance we propose to use 8 signal layers. The slots are all stepped down from low to high but we this is not a requirement this can be in a random order at the discretion of the designer. On the example on the right hand side you see that the VeCS slot have different sequences of slot depths. This is mainly determined by the pin assignment of the differential pairs.



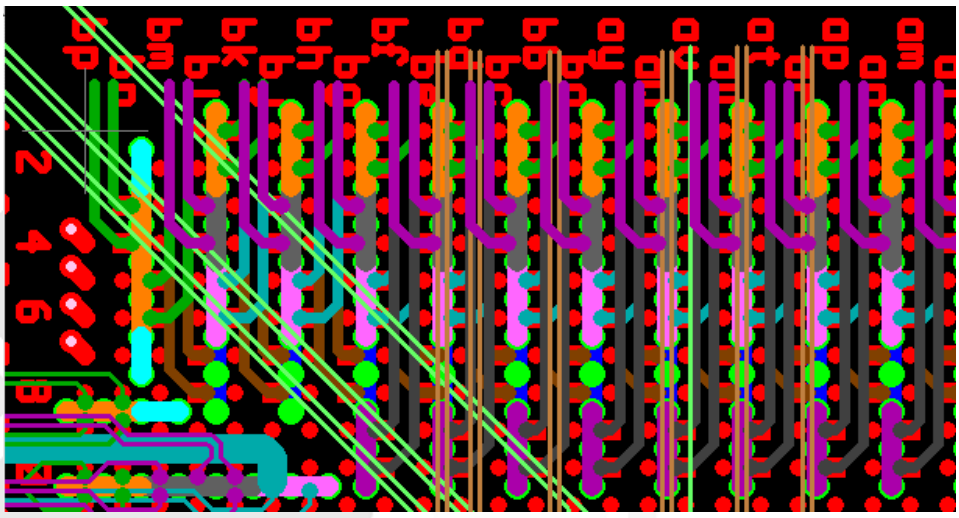
The length of the slot depth section can be varied and is mainly determined by the number of traces that can be routed in a VeCS channel. Per length of slot depth section a number of connections can be made. More connections per section will not help when there is no space for routing.

The image below shows a routing layer in purple connection to the vertical slot section in the grey colour. As demonstrated you can rout directly underneath the orange coloured slot creating extra separation between signal pairs.

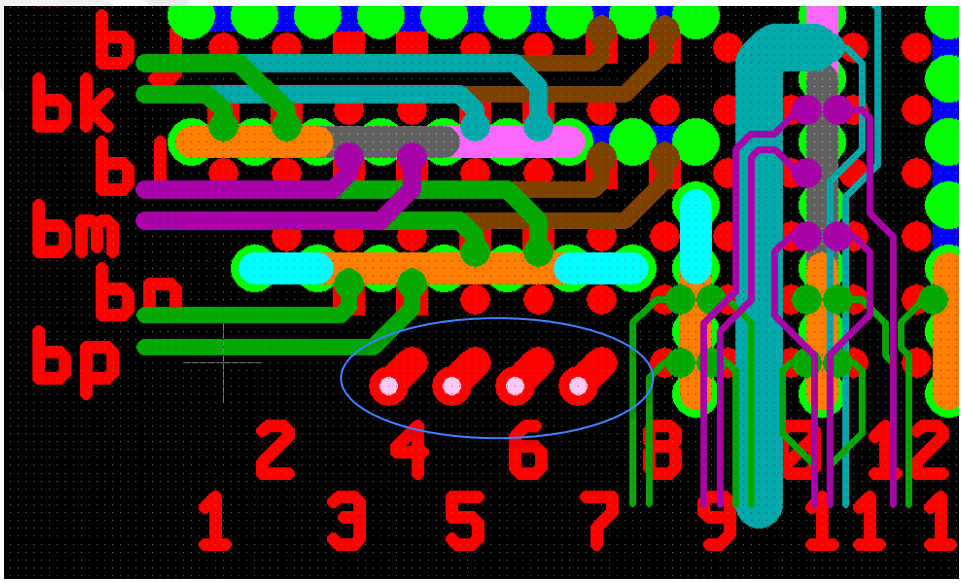


We are using 0,1mm trace width and 0,1mm spacing for the bank section. This will yield a 5 trace routing channel on its most critical position. Further in this document we show the exact design rule dimension of the complete structure.

For the high-speed SERDES section we use a single pair in the VeCS slot and can use much wider traces that we will show further in this document. We have a good separation between the slot and trace edge resulting in good plane coverage for the signal. In total we need 5 signal layers to complete the critical section. With 5 signal layers we have also 5 slot depths.



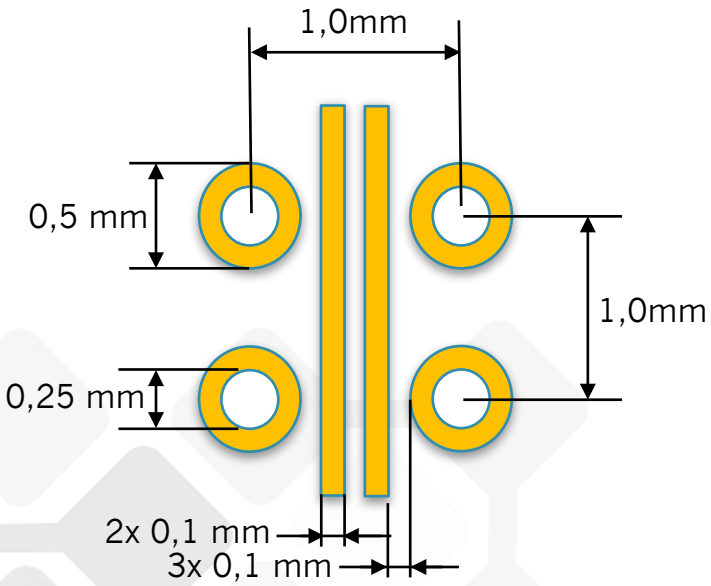
In the image above you can see that we run traces from the banks through this section. The SI engineer needs to determine if this is acceptable. The layers are all shielded and the connections will not penetrate the layers below.



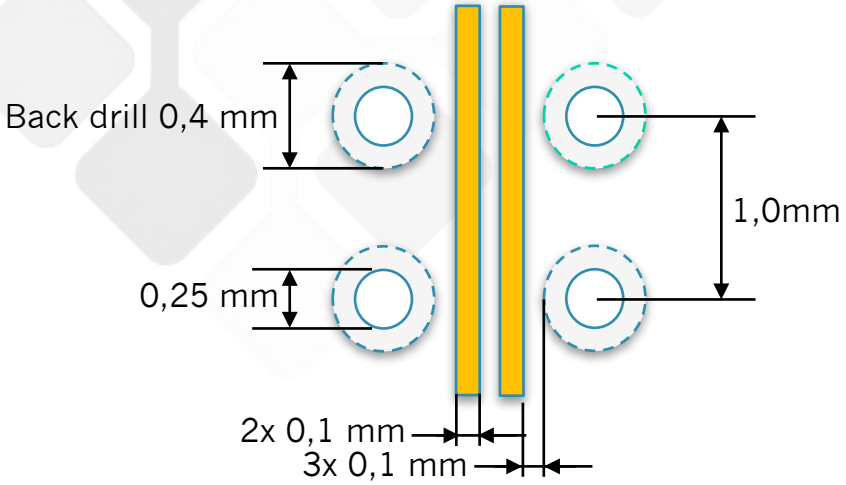
As the previous image is shown we have 4 dog bone via connections to non critical signals. VeCS can be used as well but we want to demonstrate that VeCS and traditional technology can be mixed.

Traditional /current through hole design rules

The following section is showing the design rule for high end via-hole set-up. The drill hole size in this example is



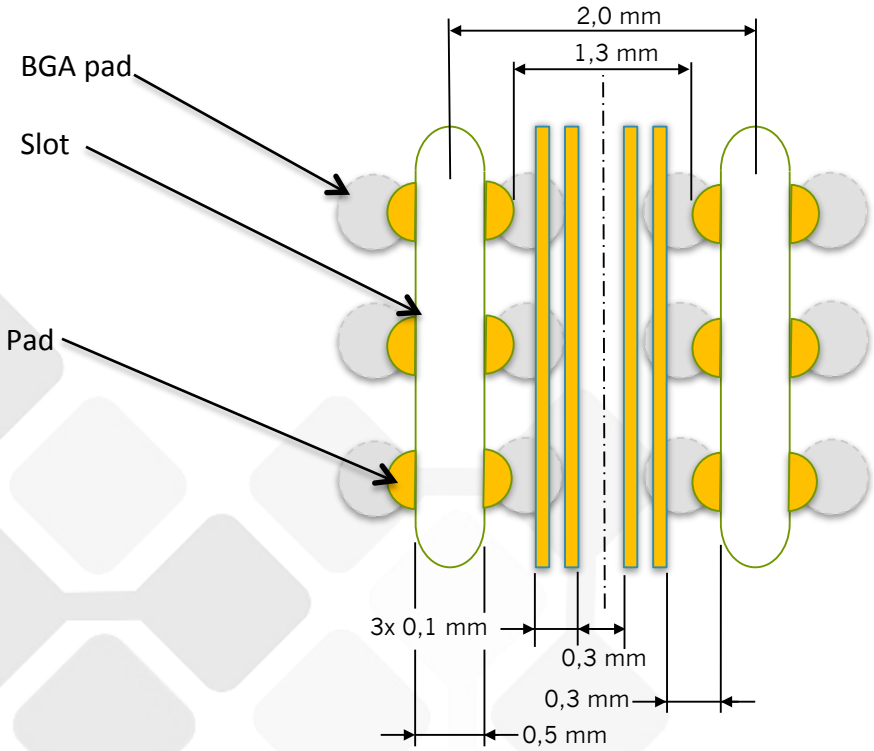
The back drill design rule is shown in the following section.



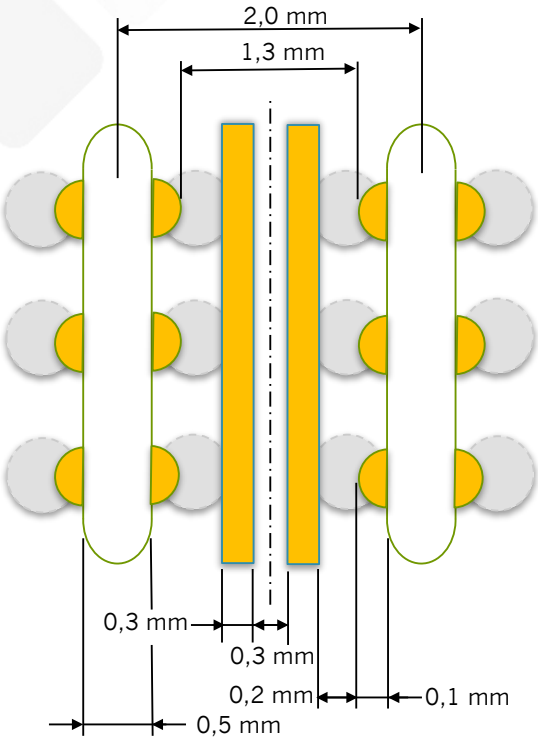
To increase the separation between the back drill and the traces the drilled hole size is reduced to 0,2mm in order to reduce the back drill diameter to 0,35mm and increase the trace to back drill spacing.

Two differential pairs in a 2.0mm pitch VeCS slot

The pairs consist out of a 0,1mm wide trace and a spacing of 0,1mm.
The separation between the pairs is 3X the spacing of the pair it self.



As an alternative we can run a single differential pair between the slots as shown in the following example reducing the DC loss of the pair.



Stack-up

To complete the fan-out of the Xilinx 2892 chip we need the following set-up when using VeCS technology as shown in the previous section.

- 8 signal layers
- 9 reference layers
- 5 voltage and GND layers
- 2 outer layers

A total of 24 layers.

This is only for the fan-out, depending how the package is positioned on the board there might be more layers required.

Separation of signals

In respect to the high speed SERDES lines and how they are routed to the opposite side it could be chosen to route only the SERDES lines on separate layers in respect to the rest of the connections (banks).

We need 4 layers for the high speed SERDES signals. Including the reference layers this would add to 9 layers extra. As a good stack-up is balanced we propose the following set-up:

- 12 signal layers
- 13 reference layers
- 5 voltage and GND layers
- 2 outer layers

A total of 32 layers.