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Connection to the Next Level

Application note – DRAFT VERSION

Transparent Stitching with VeCS-2

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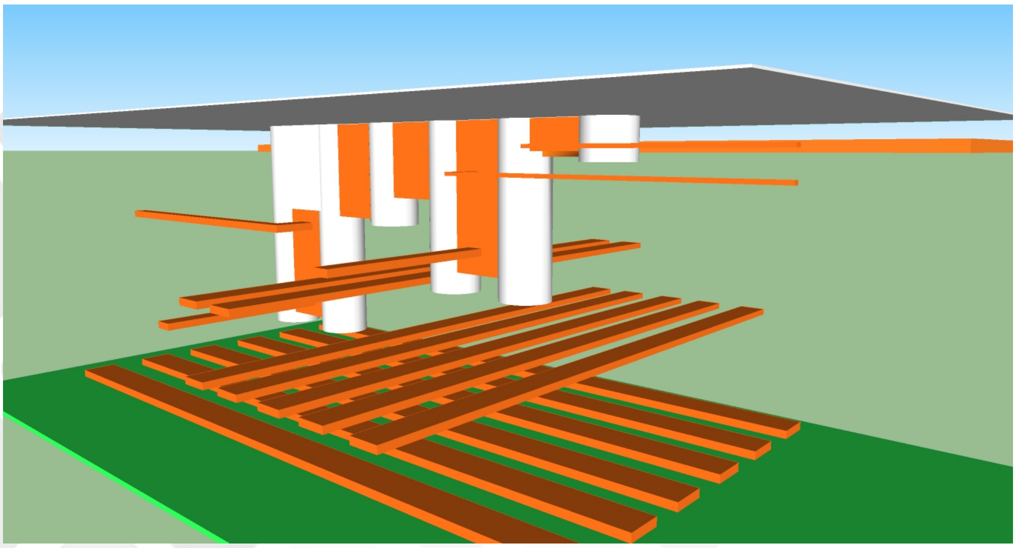
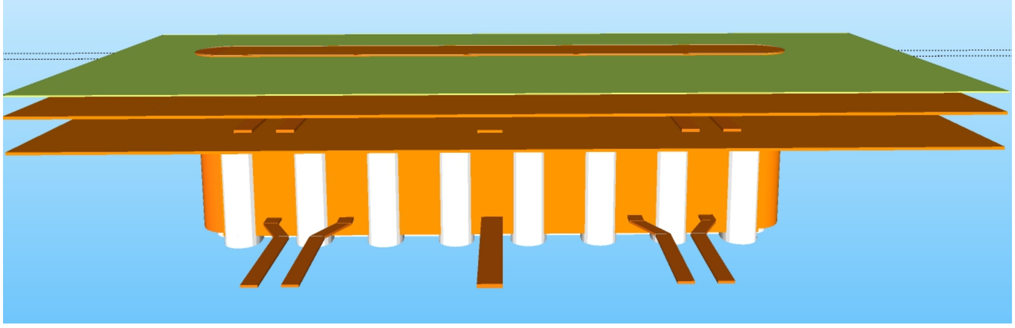
The objective of this document is to demonstrate the possibility of using a stitching element as an alternative to the point to point connections that are used with traditional via technology. Point to point connections have the best performance in terms of signal integrity; one via less in the connection that distorts the signal. A via is a mainly a capacitive element that causes signal loss / dispersion.

This study focuses on developing a layer transition element that minimises the loss and dispersion. We will use VeCS-2 technology (blind/hybrid) construction as shown in the figure below.



The advantage of using a stitching via is that we can use "traditional" orthogonal routing that is very efficient in signal layer utilization.

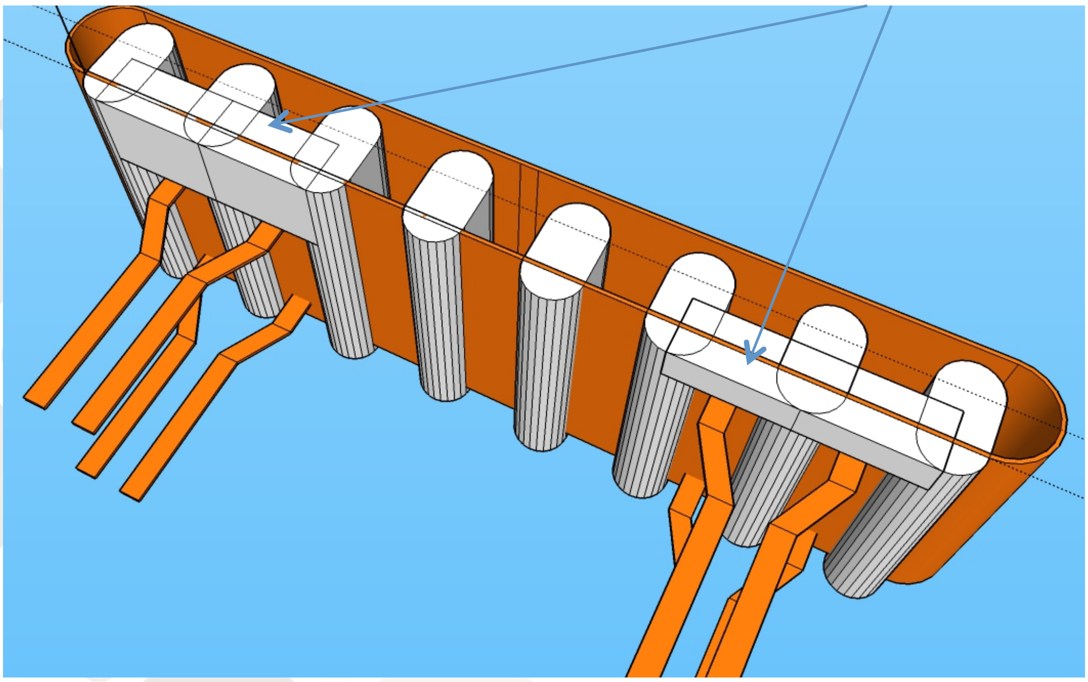
For the simulation of the stitching element we have set-up the following element; a VeCS-2 (blind) element 8 connections where we have 7 connections on one side and a GND reference on the opposite side of the slot creating a reference to the 7 connections. For visibility purposes we have not drawn all reference layers.



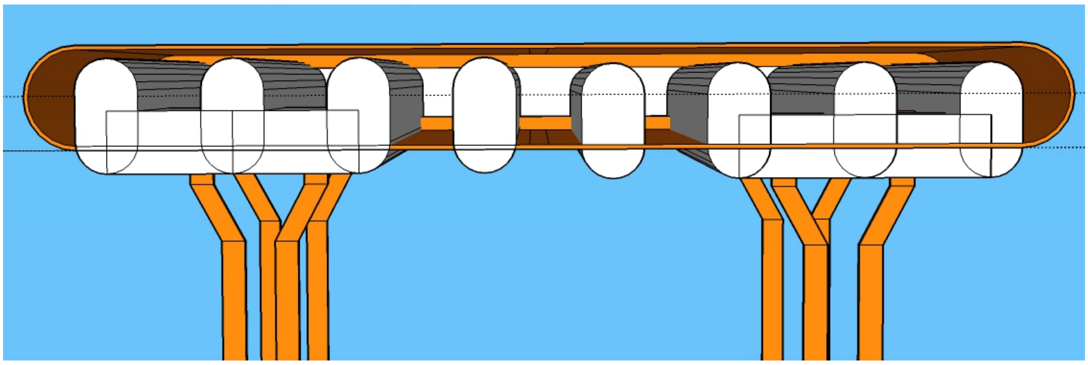
The 7 connections consist out of:

- Differential pair
- GND (purpose shielding)
- Single ended signal
- GND (purpose shielding)
- Differential pair

The GND reference is creating controlled impedance for the differential pair. The topside of the differential pair VeCS section is back routed to minimise

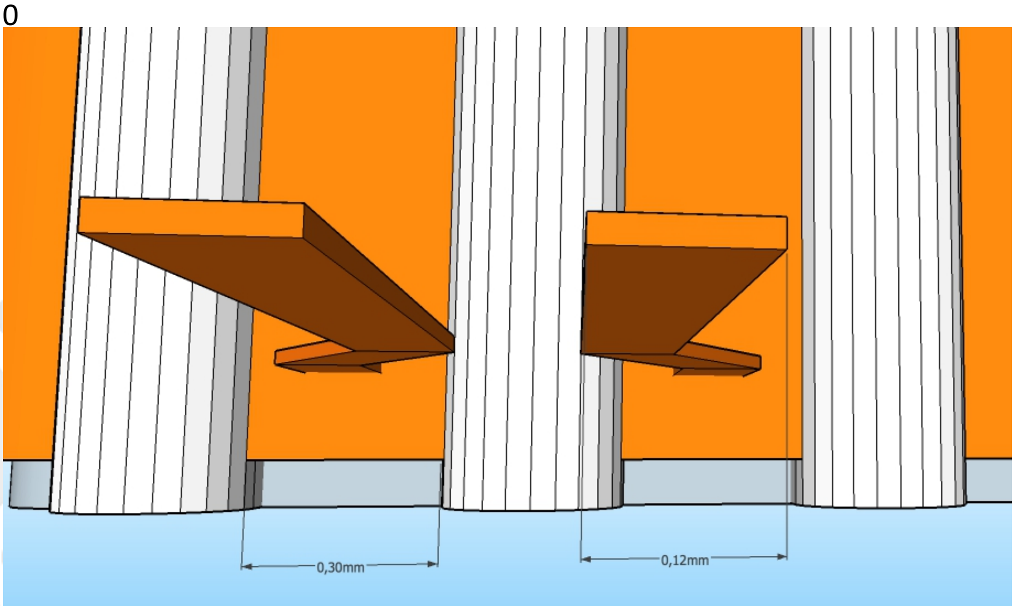


dispersion. In this image we also show the 2nd route features. The dimension of the routerbit used for 2nd route, top back route and bottom route are 0,3mm. Alle this routing is done in one and the same process step.

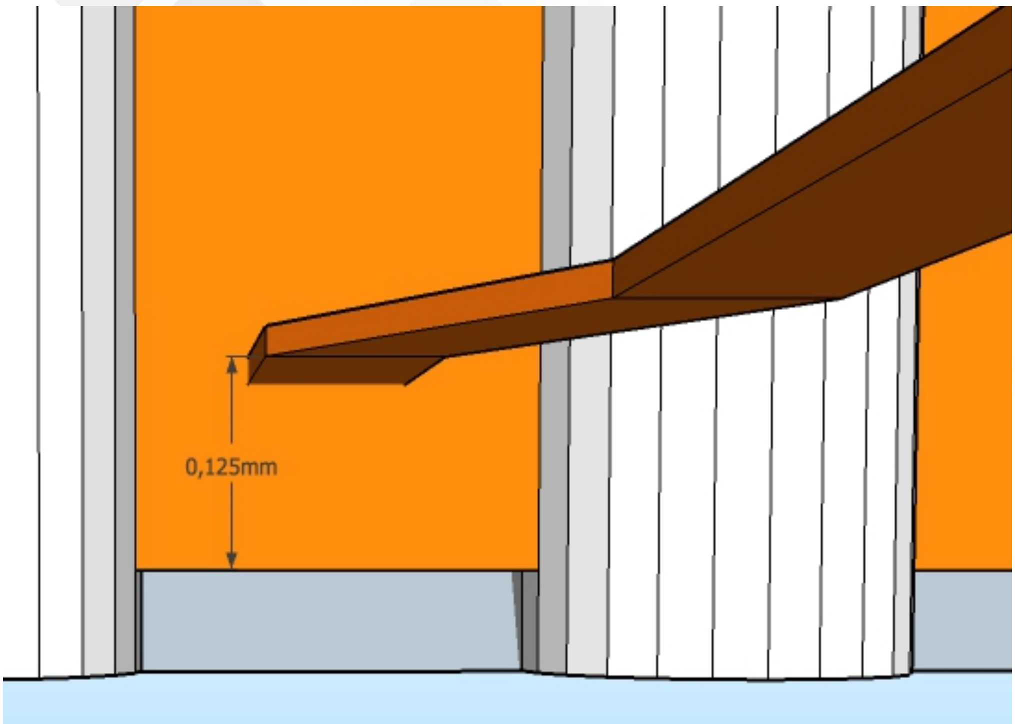


The element created is setting up a buried microstrip for the differential pairs and the single ended trace.

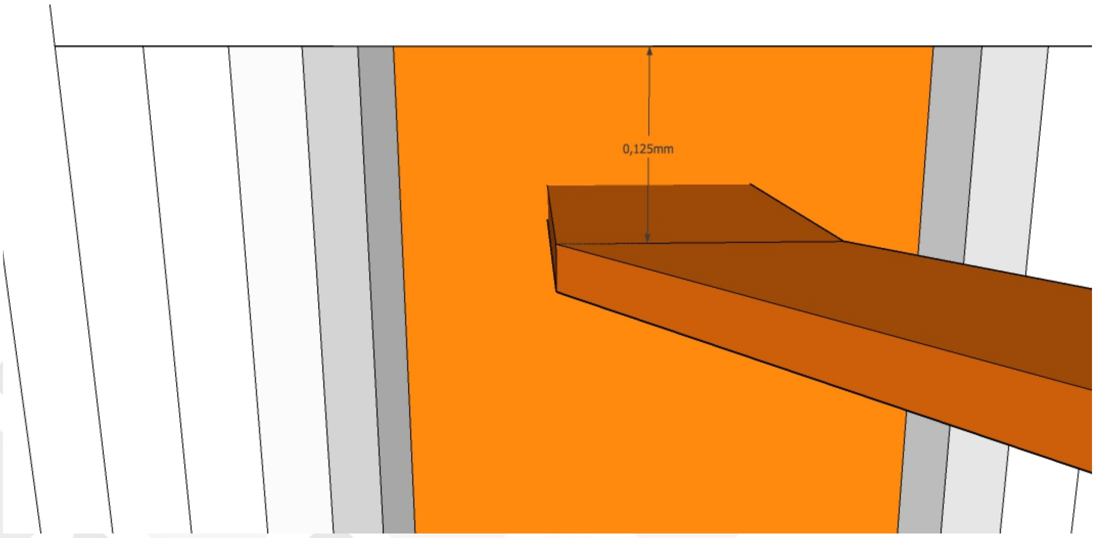
The trace width used in this example is 0,12mm, depending the stack-up this can be tuned to the required differential impedance.
The vertical trace width is 0,30mm. This will yield in a buried microstrip construction an impedance of ±110ohm (ZOdd). We took in account a Er of 4.0 for the slot filling material.
0



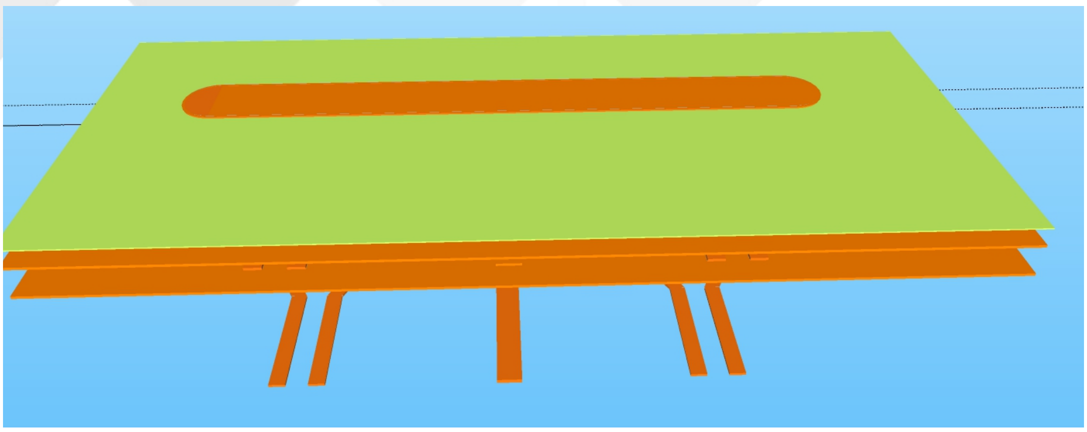
The stub length is defined by the length below the trace and the part of the slot that is left over after removing the bottom of the slot as shown in the follow image. We have set a maximum stub length of 0,125mm+0,1mm=0,225mm on the bottom side.



On the topside we have a stub length of maximum 0,125mm, here we don not have to include the 0,1mm bottom side of the slot.



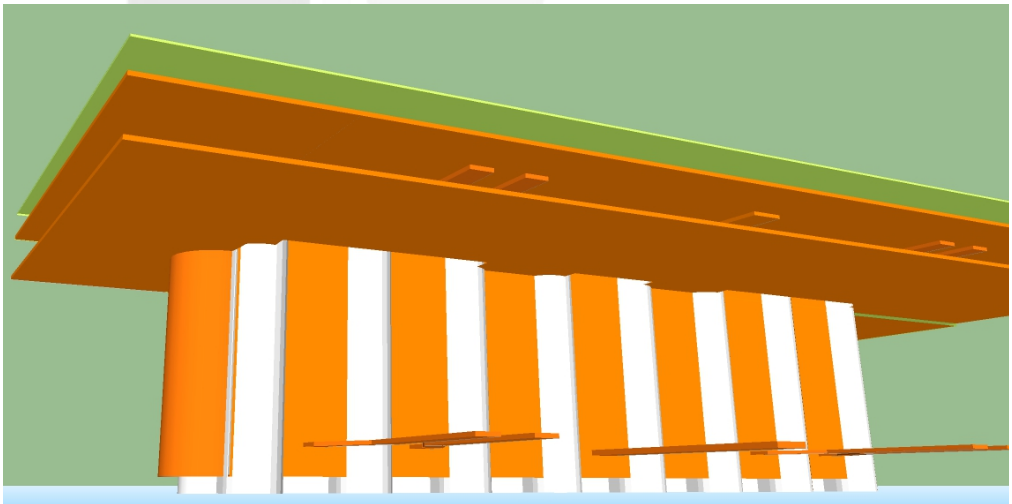
The top side of the slot is overplated (after filling the trench with a dielectric) as shown in the image below.



The stack up for this test vehicle is as follows:

Layer	Type	Dielectric	Thickness [um]	Trace width [um]	Spacing [um]	Impedance Zodd
1	Outer layer	Cu	50			
	Dielectric	Er 4.0	200			
2	GND	Cu	35			
	Dielectric	Er 4.0	200			
3	Signal	Cu	18	120	120	100 Ω
	Dielectric	Er 4.0	200			
4	GND	Cu	35			
	Dielectric	Er 4.0	1000			
5	GND	Cu	35			
	Dielectric	Er 4.0	200			
6	Signal	Cu	18	120	120	100 Ω
	Dielectric	Er 4.0	200			
7	GND	Cu	35			
	Dielectric	Er 4.0	200			
8	Outer layer	Cu	50			

The dielectric in the center of the board (thickness 1.0mm) can be varied to adjust the vertical trace length to determine the influence on the signal performance.

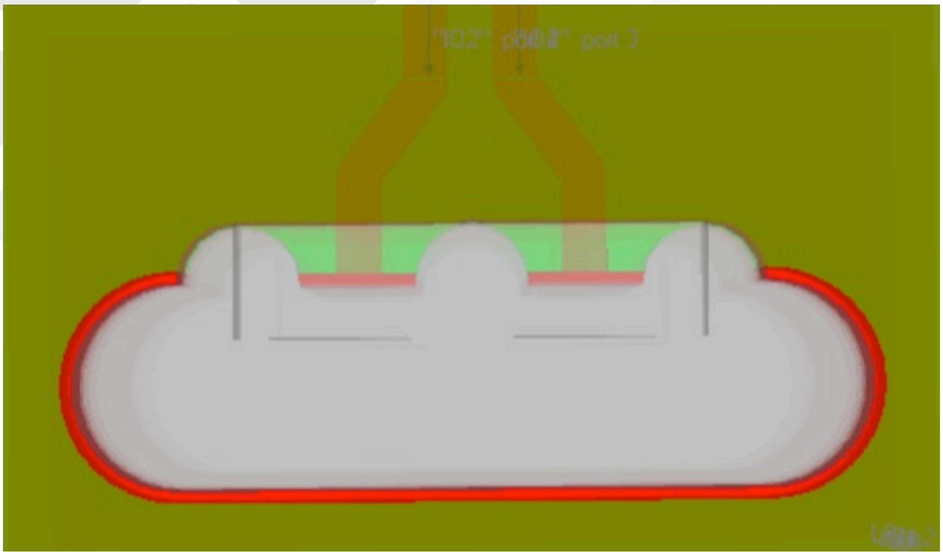


Signal integrity analysis of the VeCS stitching element

Escaping out of a connector or BGA array is one complexity factor next to that is the options to create layer transitions to avoid the point-to-point connections on the same layer. To minimize signal distortion/reflection p2p connections are used in favour of via layer transitions. In this section we analyse the SI performance of layer-to-layer transitions using VeCS-2 technology.
Enabling the use of layer transition with little reduction in Si-performance of the transmission line will simplify the routing of a lot of designs. This reduces the complexity of the design e.g. Layer reduction, eliminating sequential build-ups, etc.

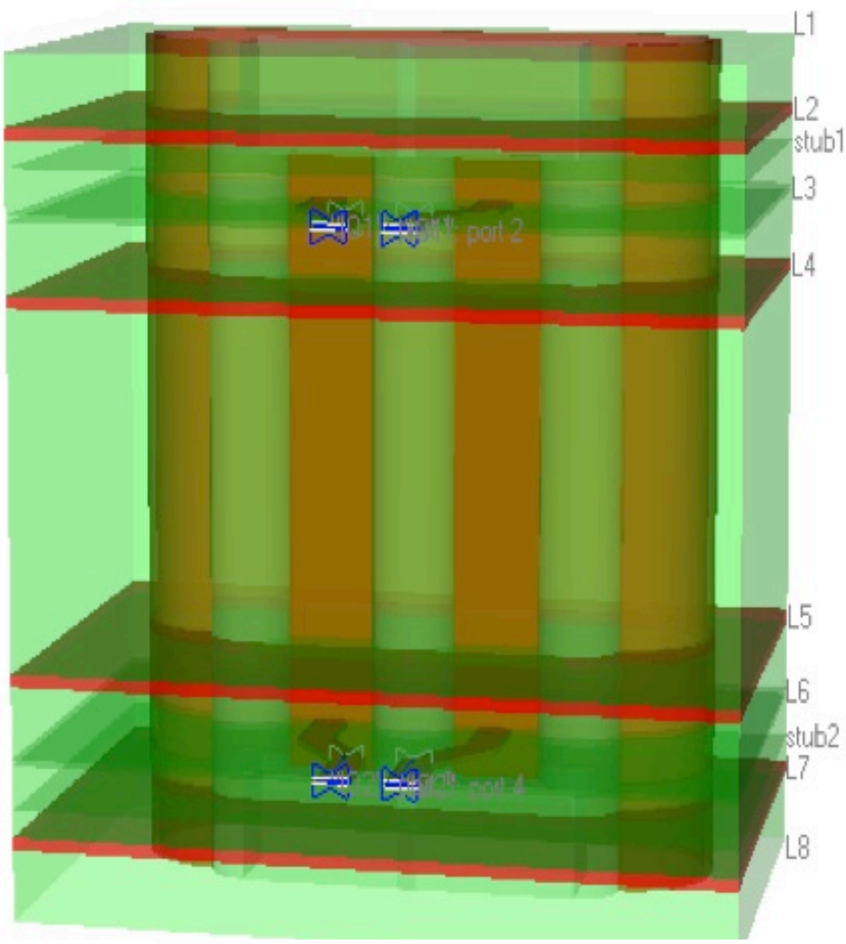
For the SI performance analysis we used “Simbeor THz 2017.01” with thanks to Yuriy Schlepnev (Simberian) for translating our VeCS design in the analysis and simulation tool.

From the mechanical VeCS-2 design principles the following VeCS element was created. We use one differential pair per VeCS where the rest of the element is shielded as shown below in the top view.



We created an 8 layer stack-up targeting a 95 ohm differential impedance as shown in the 3D view as shown in the image below.
When we perform the 2nd route we clean the bottom section, we create the vertical traces and remove the stub on the top of the VeCS traces. This is all can be done in one cycle.

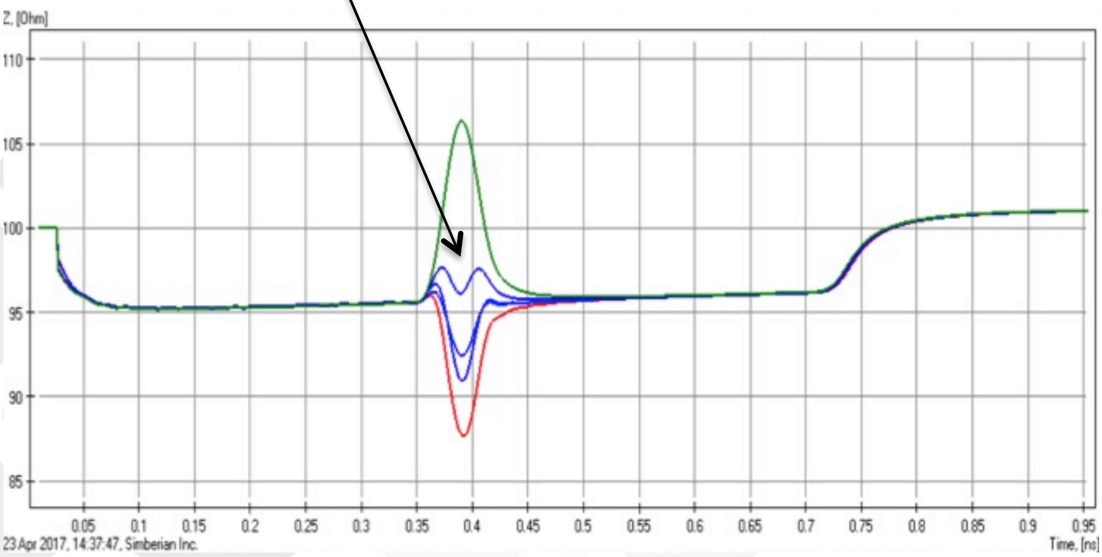
What is not shown is the cap plating we prefer to have on the other layers shielding. This has little influence on the Impedance of the vertical traces.



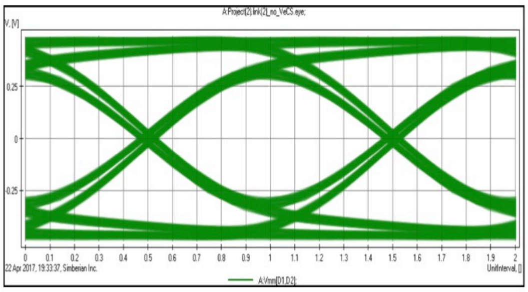
Layer 3 and 7 and the signal layers, the other layers are reference.

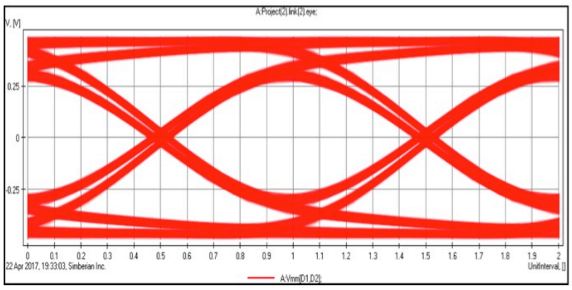
The first objective in the analysis was to perform a Time Domain simulation and tune the trace width, anti-pad sizes such that we create the smallest distortion possible.

We started with a traditional capacitive response as expected form a layer transition (e.g. via through hole) and started to tune the VeCS element such that we got close to a flat line. More modification turned it into a inductive element.

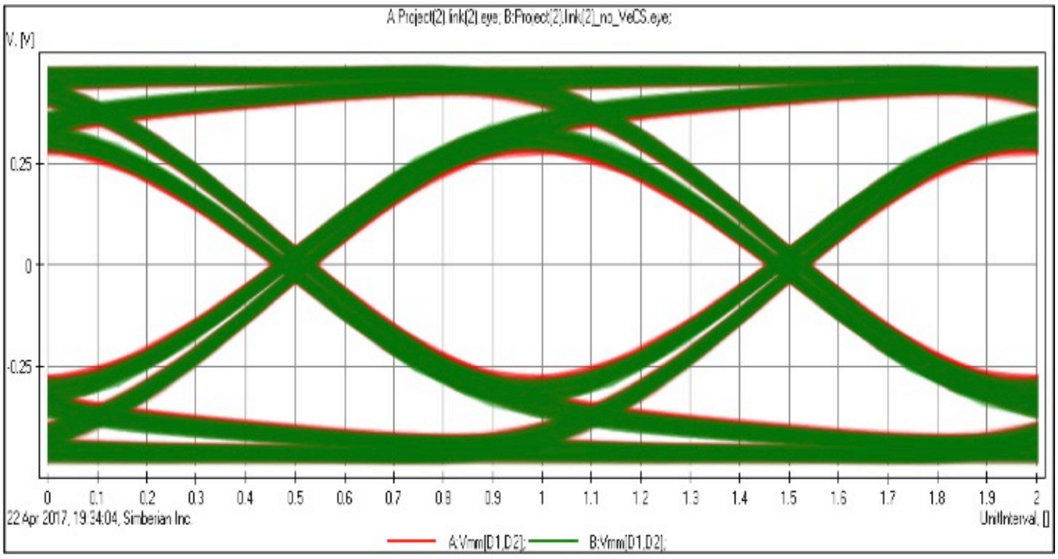


We used the results of the TD simulation for perform the 30Gb/s bitstream eye-diagram simulation. In green below the reference transmission line without the tuned VeCS element and in red the transmission line with a tuned VeCS layer transition.





In the following eye diagram we superimposed the eyed-diagram for the transmission line without VeCS (green) on the eye-diagram of the transmission line with the VeCS element in red.



The eye is a bit more closed when using the VeCS, it is a marginal 0,516V versus 0,539V for the transmission line without VeCS. Details of the two eye-diagrams are listed in the table below.

Eye Diagram Parameter	Transmission line Without VeCS	Transmission line With VeCS
Eye Level Zero	-0.383742 [V]	-0.377428 [V]
Eye Level One	0.382528 [V]	0.377346 [V]
Eye Level Mean	-0.00182348 [V]	-0.000614657 [V]
Eye Amplitude	0.76627 [V]	0.754774 [V]
Eye Height	0.538959 [V]	0.516313 [V]
Eye Width	0.902439 [UI]	0.897118 [UI]
Eye Opening Factor	0.703354	0.684063
Eye Signal to Noise	6.04823	5.68955
Eye Rise Time(20-80)	0.504472 [UI]	0.512165 [UI]
Eye Fall Time(80-20)	0.505318 [UI]	0.512579 [UI]
Eye Jitter(PP)	0.097561 [UI]	0.102882 [UI]
Eye Jitter(RMS)	0.0250763 [UI]	0.0276838 [UI]