NextGIn

Connection to the Next Level

Application note // DRAFT

Fan-out 0,50mm stapitch BGA using VeCS.

Joan Tourné
NextGIn Technology BV

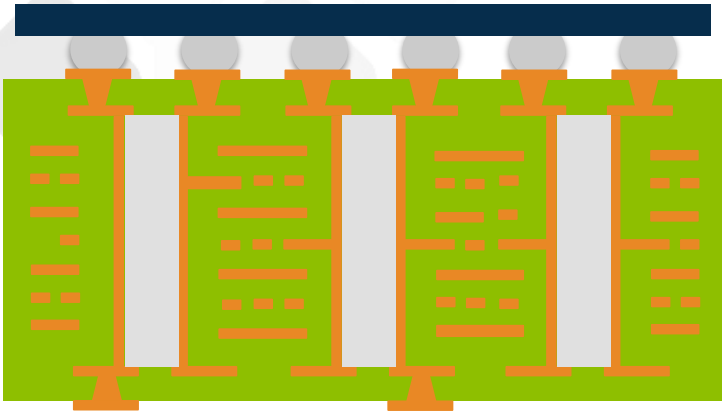
February 27th 2017

In this document we describe the use of VeCS in a high I/O count 0,50mm pitch area array type package as shown in the next diagram. The I/O is 54x54 (2916),
This means a depth of complexity (DOC) of 14 rows deep assuming a 50% ratio of signal versus power and ground.

With current through hole technology routing this device is not an option. The drill hole size of 0,25mm and a annular ring of 0,1mm yields only a routing space of 0,1mm.
The objective here is to use differential routing of minimum 0,1mm trace width. The minimum required space in the routing channel is 0,5mm (2 traces and 3 spaces of 0,1mm).

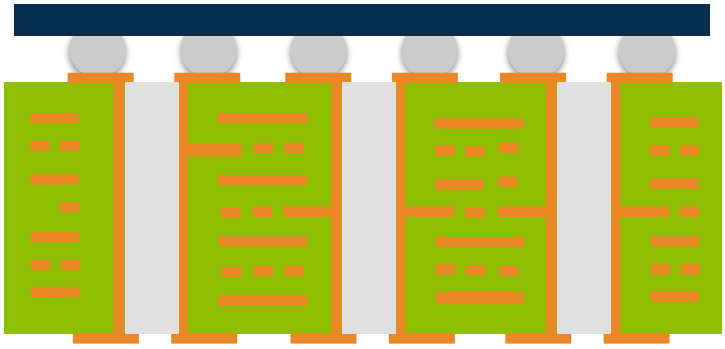
In this document we want to apply a VeCS technology on this package and demonstrate a fan-out. Application the VeCS slots to the surface parts of the pad will be placed on top of the filled and over plated slot. Flatness of the pads even for such a small device will be major criteria for a reliable assembly process. If flatness is a criteria the VeCS can be buried as shown in the figure below. After the core is manufactured measurements should be taken to determine the flatness. At that point one can then determine if flatness is within specification.

In the following images we show two stackup, one using a 1+n+1 built and a stack-up using a single lamination cycle.
As shown in the drawing the VeCS element is filled with a via-filling material and (partially) over plated to form the landing pads for the microvias. The drawings are not to scale.



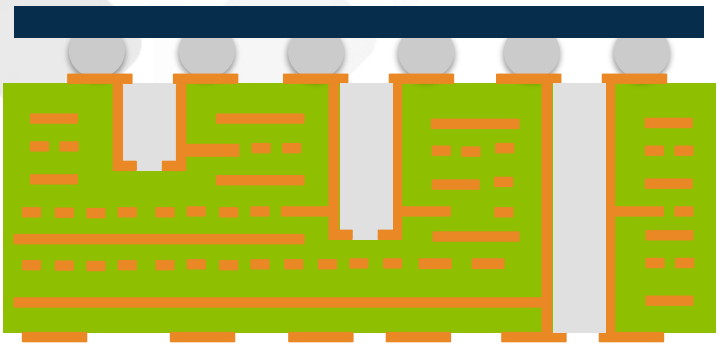
This document is property of NextGIn Technology BV.
VeCS technology patented.

Following the stackup built in a single lamination cycle. Without the microvias on top of the VeCS.



For the fanout it will not make a difference if the a microvia stack-up is used or a straight built. The choice will be more determined by the creating of the outerlayers and the flatness of the pads.

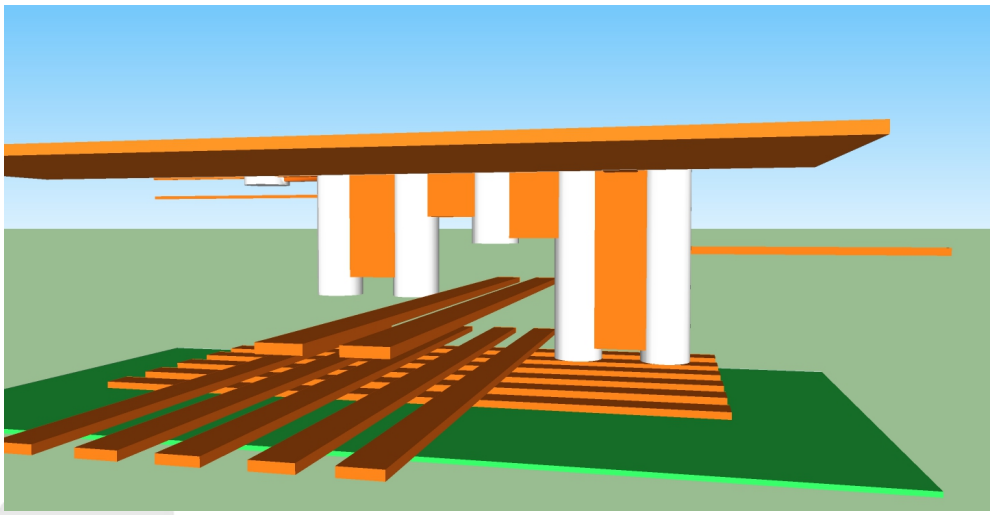
In the following image we show a cross section of a stack-up in which we use the VeCS-2 technology. The advantage of VeCS-2 is that we can plate high aspect ratio blind structures. Aspect ratio's in blind holes are typically limited to 1:1, hole depth versus hole diameter. In VeCS-2 we can create reliable structures of 10:1 (tested and proven). We anticipate that we can plate AR of 20:1 in the very near future. The length of the slot will be a variable in the criteria of plating a blind slot. Hybrid slots that go all the way through the board for one section of the slot where other parts of the slot step down to a certain layer.



Routing with VeCS-2 has advantages, the space under the slot is free of blockages and traces can be routing in all directions. This can result in larger spacings between differential pairs or can result in layer reduction.

This document is property of NextGIn Technology BV.
VeCS technology patented.

In the next images we show the use of VeCS-2 technology in 3D. In



comparison with traditional Vias or Microvias the possibilities in routing and slot formation have not been fully explored. We will keep on developing, designing and building these products to learn the opportunities of the technology.

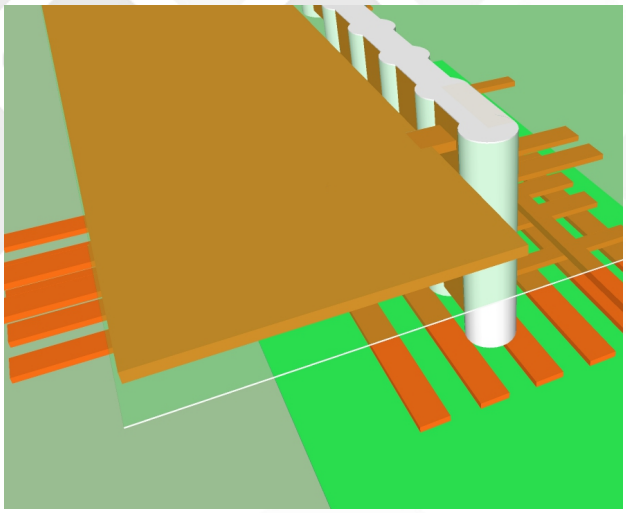
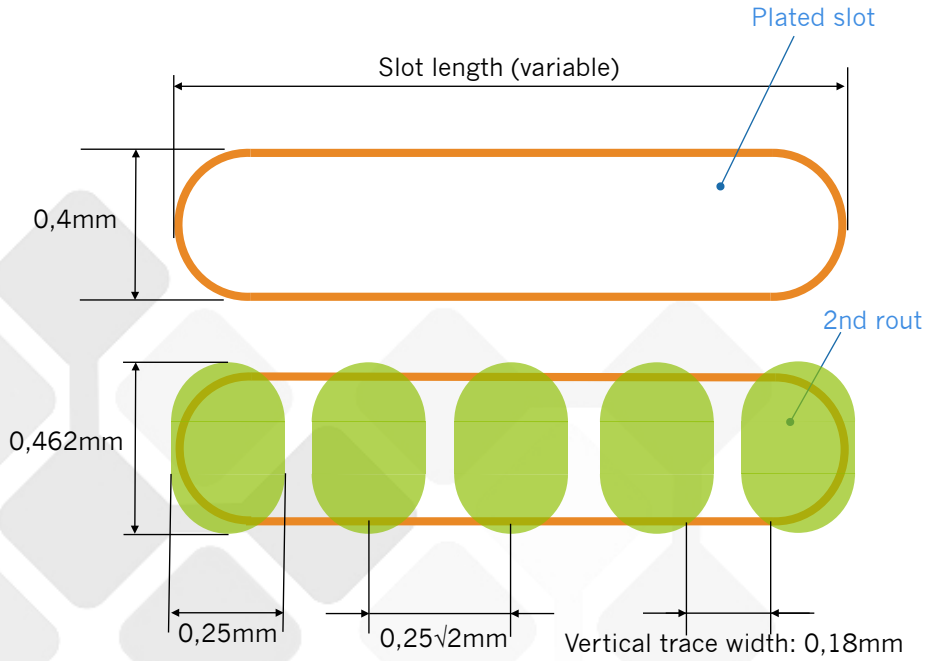


Figure shows the connection of a copper plane to the VeCS element.

This document is property of NextGIn Technology BV.
VeCS technology patented.

Dimensions

In the figure below we show the dimensions of the diagonal placed slot. The dimensions of the horizontal and / or vertical placed slots are different from the 45 degree diagonal slot.



Same set-up for the orthogonal placed slot. The vertical trace width is getting wider. For Si purposes the trace width between diagonal and orthogonal traces should be equal. This can be achieved by making the 2nd rout wider to create a vertical trace that is equal for both slots.

The position of the landing pad or BGA pad against the slot position is shown below.

This document is property of NextGIn Technology BV.
VeCS technology patented.

Example

The example fan-out as shown in this section is based on a 0,5mm 54x54 footprint. We used a orthogonal and diagonal slot position. Note that is a generic and used as a example. Other patterns can be used as well.

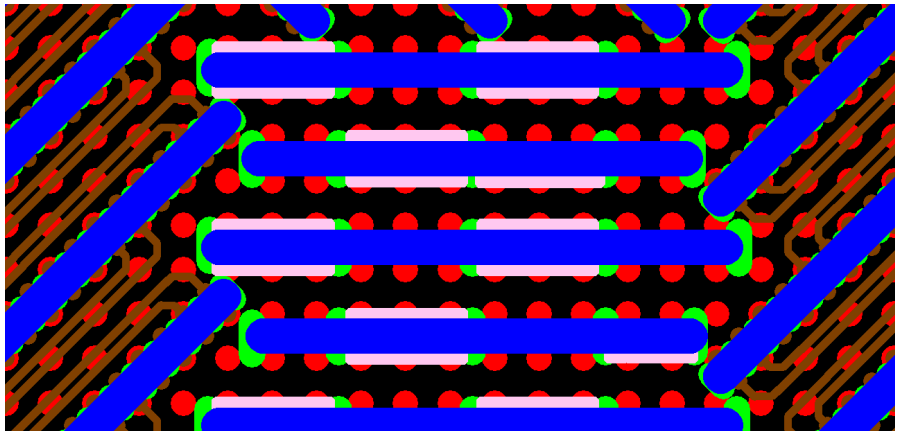
The routing channel and utilization for the two different slot types listed in the following table.

Slots orientation	Routing channel width	Spacing trace to slot	Trace width	Spacing	# traces
Orthogonal					
Differential	0,6mm	0,187mm	0,075mm	0,075mm	2
Single	0,6mm	0,25mm	0,1mm	-	1
Diagonal					
Differential	1,026mm	2x 0,185mm	0,075mm	0,075/0,21mm	4
Single	1,026mm	2x0,175mm	0,075mm	0,075mm	5
Single	1,026mm	2x 0,2mm	0,1mm	0,1mm	2
Single	1,026mm	2x0,2mm	0,12mm	0,12mm	2

The next image shows the top view of the center of the 54x54 0,5mm BGA. We assumed the centre of the BGA is connected to GND and supply voltages. The design is made in a CAM program called Viewplot.

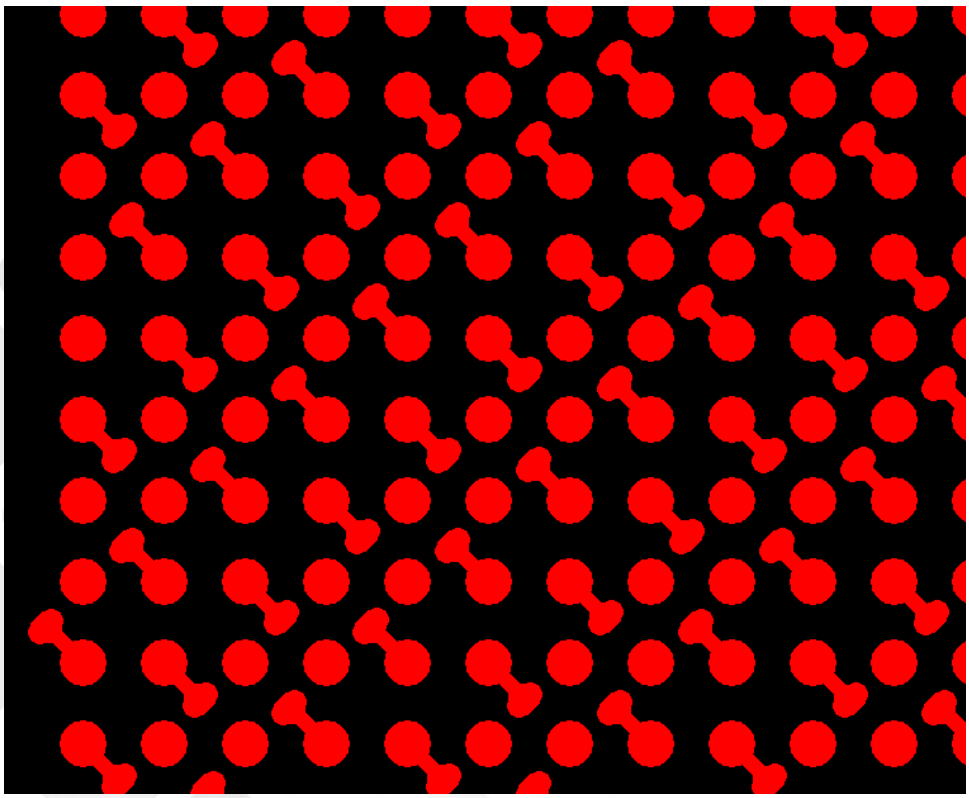
We show the traces in the routing channel (brown) and the slots in blue (0,4mm wide). We used 2 differential pairs each of 0,075mm with 0,075mm spacing and maximized the spacing between the pairs to 3x the trace width.

The red layer is the outerlayer or if a microvia cap is used the first innerlayer with the microvia landing pads.
The green oblong pads are the second route slots.

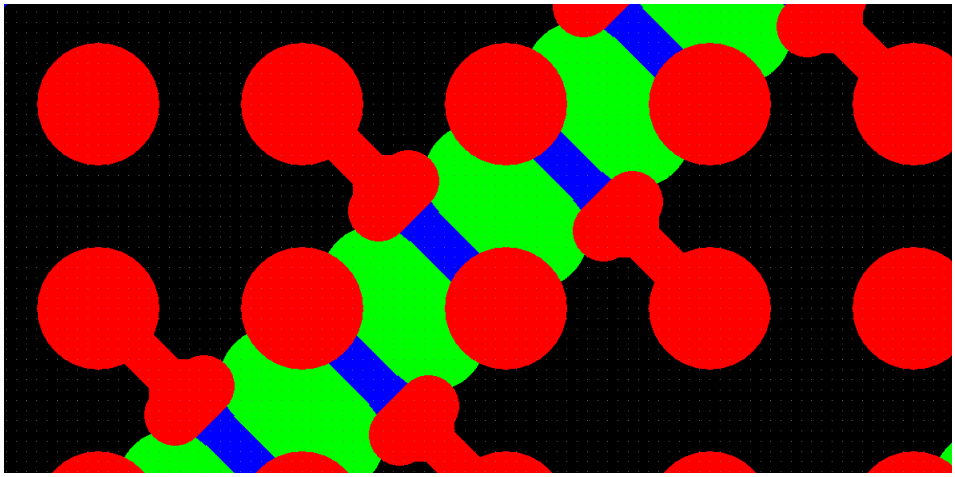


This document is property of NextGIn Technology BV.
VeCS technology patented.

The outerlayer is shown in the image below for the diagonal placement of the slots below. We use a dog bone to connect the pads between the slots to the vertical trace. The other pads are sitting on top of the filled slot. Again, other patterns can be used, so can the pads on top of the slot pulled to the area between the slots and connect those pads using a microvia.



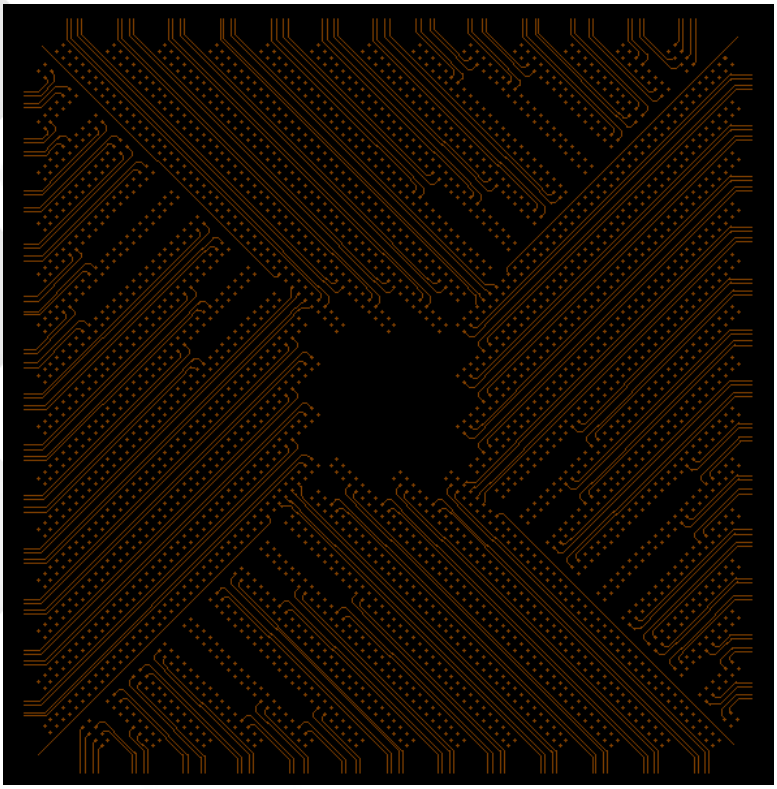
To get a better understand how the images/layers relate we show in the next image the connection of the red layer to the vertical trace (blue slot). The green oblong pad is the 2nd rout.



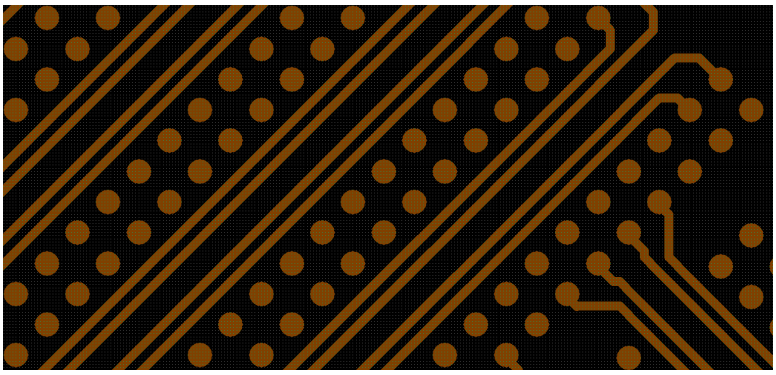
This document is property of NextGIn Technology BV.
VeCS technology patented.

On the internal layer we used 2 coupled traces of 0.075mm and a spacing of 0,075mm. The spacing between the pairs

This BGA fanout example is academic and we assumed a 50% pin to GND/VCC ratio. The diagonal placement means that the DOC (Depth Of Complexity) is 40 * 50% is 20 pins per row to be routed to the outside. This equals for 2 slots with 20 pins in a total of 40 signal pins to be routed between two slots.
4 slots per channel equals in signal 10 layers. Assuming a single stripline construction means 11 GND/reference layers. With extra voltage layers this would result in a 28 – 30 layer construction.

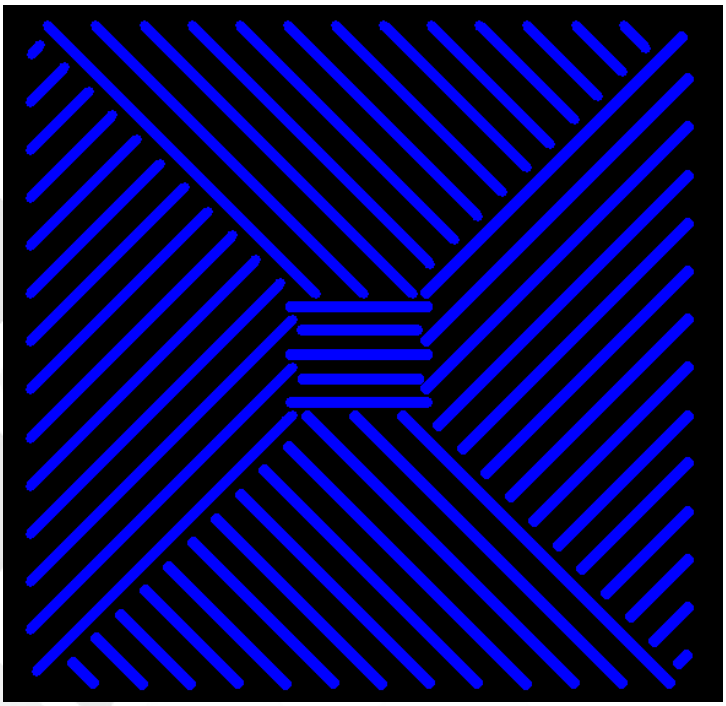


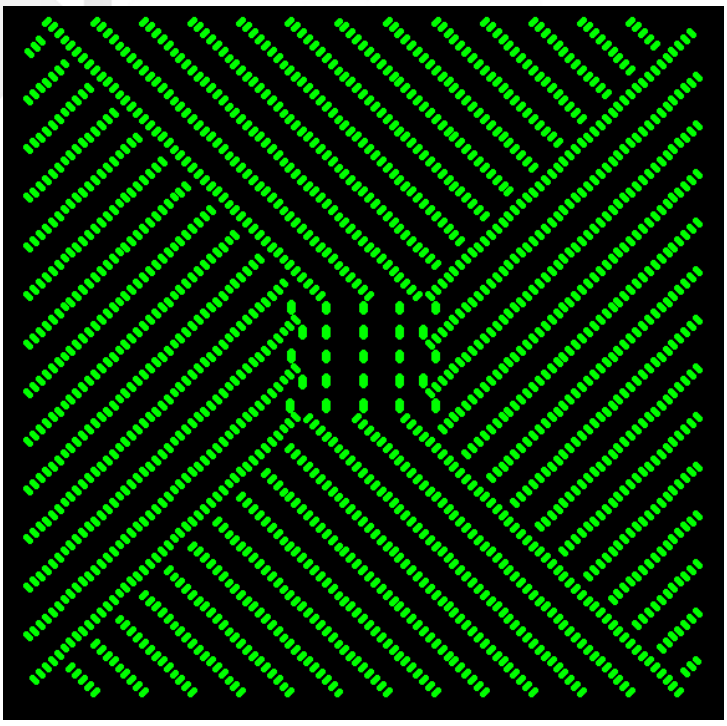
A larger image of the internal layer is shown below.



This document is property of NextGIn Technology BV.
VeCS technology patented.

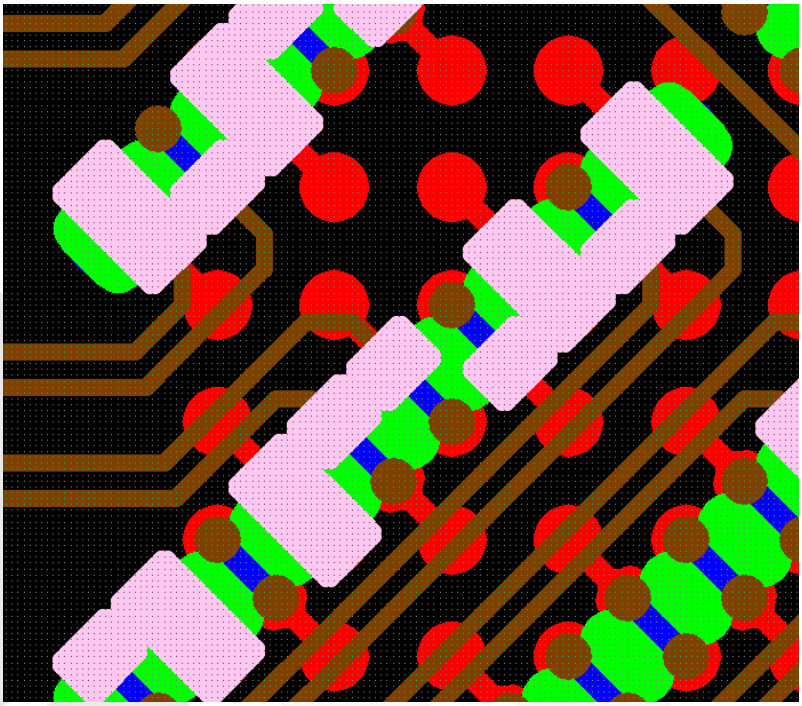
We have Gerber data available for the example design as shown in this document. This helps in understanding how VeCS technology is used.
The images below show the individual layers for the slot and 2nd rout. These layers can be supplied as Drill/Route data or as Gerber data.
We have chosen the diagonal approach with a combination of horizontal slots for the core.





This document is property of NextGIn Technology BV.
VeCS technology patented.

How the Power / GND connections are made is shown in the image below. The pink boxes are the antipads. On the positions where there is no antipad there is a solid connection to the Power/GND layer.



The use of VeCS in this application is focussed on creating more routing channel width by increasing the density of the vertical connections. We do not address the improvements that can be made in terms of signal conditioning.
The advantage in the stack-up of the VeCS core is that you can use material and dielectric thicknesses for minimizing signal loss and matching impedance. Core thickness of the first sub of the first lamination is limited to a thickness of 4mm.

As we do not have a pin assignment for this generic package we assume that the center rows and columns of the package is connected to GND and Power. We connect these pins to the internal layers using VeCS as well.

In the following design we use VeCS-1 technology where we create the slot all the way through the buried core. The slot with is 0,3mm and a 0,25mm 2nd rout to cut the plating of the slot to create the vertical trace. The vertical trace width is ±0,1 mm. The 2nd rout can be applied after Sn plating before Cu etch. Any Cu burrs from the routing will be removed during etching resulting in a clean cut.
If the high speed or sensitive analogue signals are used the traces can be routed back before the core is laminated is filled and laminated.

This document is property of NextGIn Technology BV.
VeCS technology patented.

The design as shown is an example and many more options are possible.

An option using VeCS-2 technology (blind slots) is possible but not addressed in this note. The slot width for VeCS-2 will be 0,4mm. We will address this in another application not

This application note is generic and can be adjusted to your specific needs. If you have an application / a package and pin assignment we will provide you a set-up recommendation for VeCS and stack-up.

Please contact us on info@nextgin-tech.com.

This document is property of NextGIn Technology BV.
VeCS technology patented.