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Connection to the Next Level

# Application note

*Fan-out 0,35mm staggered pitch BGA using VeCS.*

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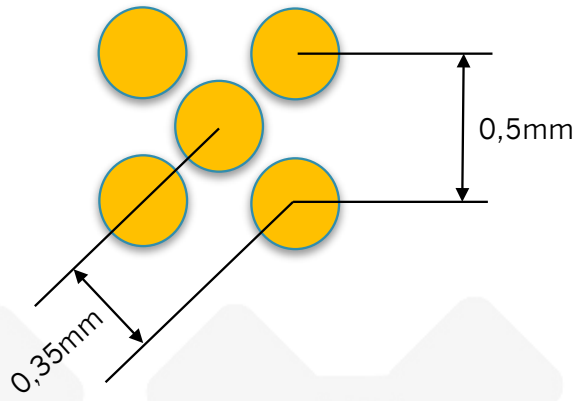
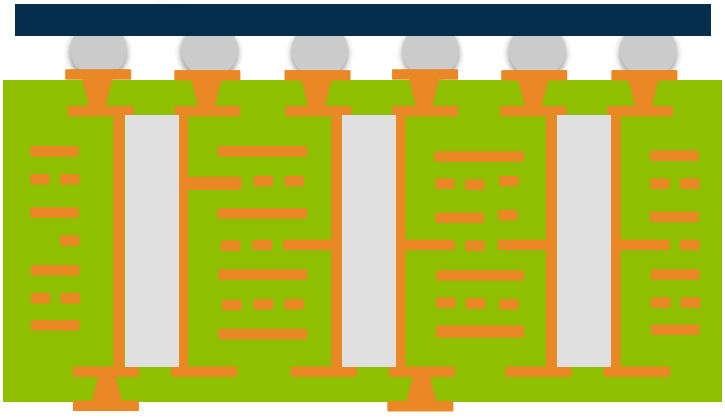
In this document we describe the use of VeCS in a staggered 0,35mm pitch area array type package as shown in the next diagram.
The package consists out of a 17x17 array (578 IO). This means a depth of complexity (DOC) of 6 rows deep assuming a 50% ratio of signal versus power and ground.




With current through hole technology routing this device is not an option. Using Microvias is an option but the pad sizes for Microvias are for advanced technology 0,2mm which means a routing channel in the 0,35mm direction of 0,15mm. This yields a track and gap of 0,05mm.

In this document we want to apply a VeCS technology on this package and demonstrate a fan-out. Application the VeCS slots to the surface parts of the pad will be placed on top of the filled and over plated slot. Flatness of the pads even for such a small device will be major criteria for a reliable assembly process. If flatness is a criteria the VeCS can be buried as shown in the figure below. After the core is manufactured measurements should be taken to determine the flatness. At that point one can then determine if flatness is within specification.
As shown in the drawing the VeCS element is filled with a via-filling material and (partially) over plated to form the landing pads for the microvias. The drawing is not to scale.



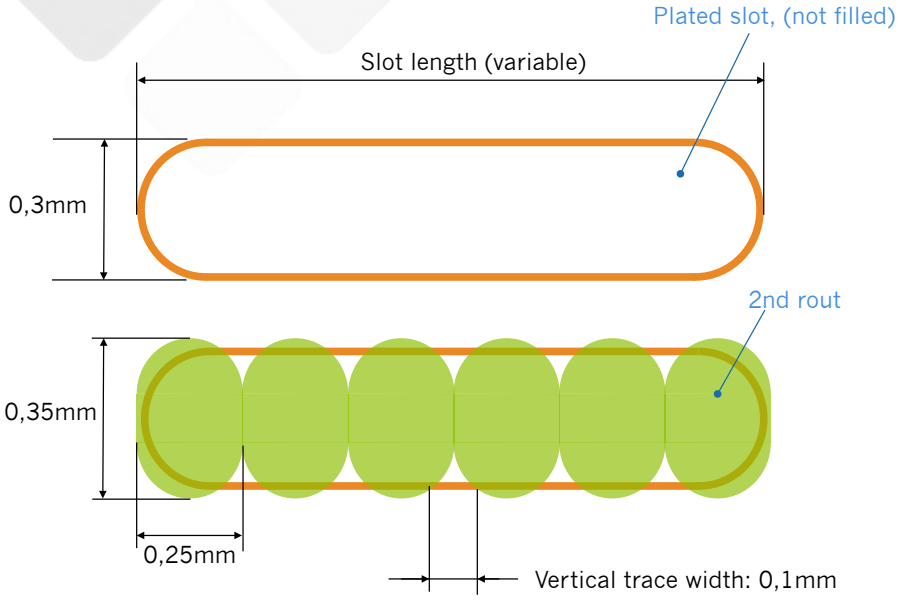
The use of VeCS in this application is focussed on creating more routing channel width by increasing the density of the vertical connections. We do not address the improvements that can be made in terms of signal conditioning.
The advantage in the stack-up of the VeCS core is that you can use material and dielectric thicknesses for minimizing signal loss and matching impedance. Core thickness of the first sub of the first lamination is limited to a thickness of 4mm.

As we do not have a pin assignment for this generic package we assume that the center rows and columns of the package is connected to GND and Power. We connect these pins to the internal layers using VeCS as well.

In the following design we use VeCS-1 technology where we create the slot all the way through the buried core. The slot with is 0,3mm and a 0,25mm 2nd rout to cut the plating of the slot to create the vertical trace. The vertical trace width is ±0,1 mm. The 2nd rout can be applied after Sn plating before Cu etch. Any Cu burrs from the routing will be removed during etching resulting in a clean cut.
If the high speed or sensitive analogue signals are used the traces can be routed back before the core is laminated is filled and laminated.

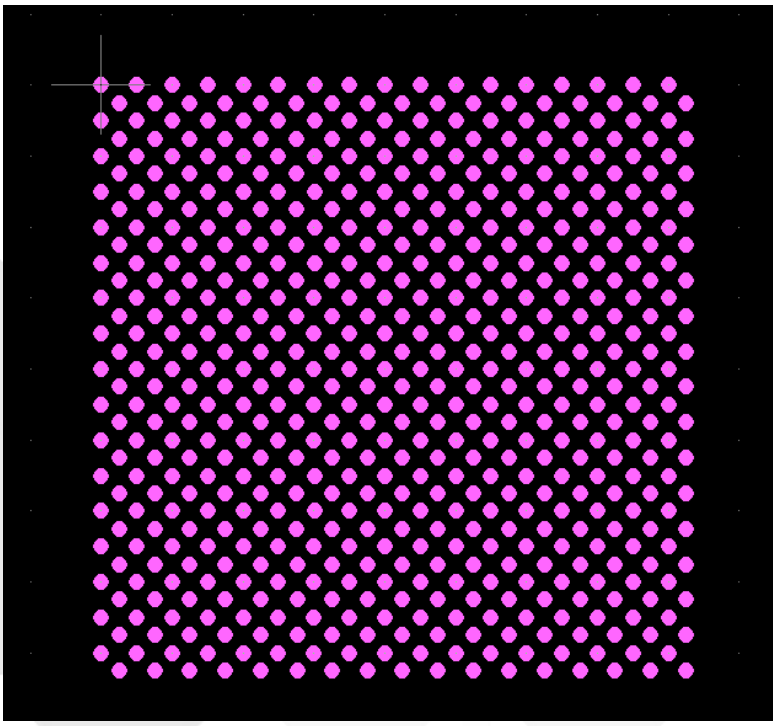
The design as shown is an example and many more options are possible.

An option using VeCS-2 technology (blind slots) is possible but not addressed in this note. The slot width for VeCS-2 will be 0,4mm. We will address this in another application note.

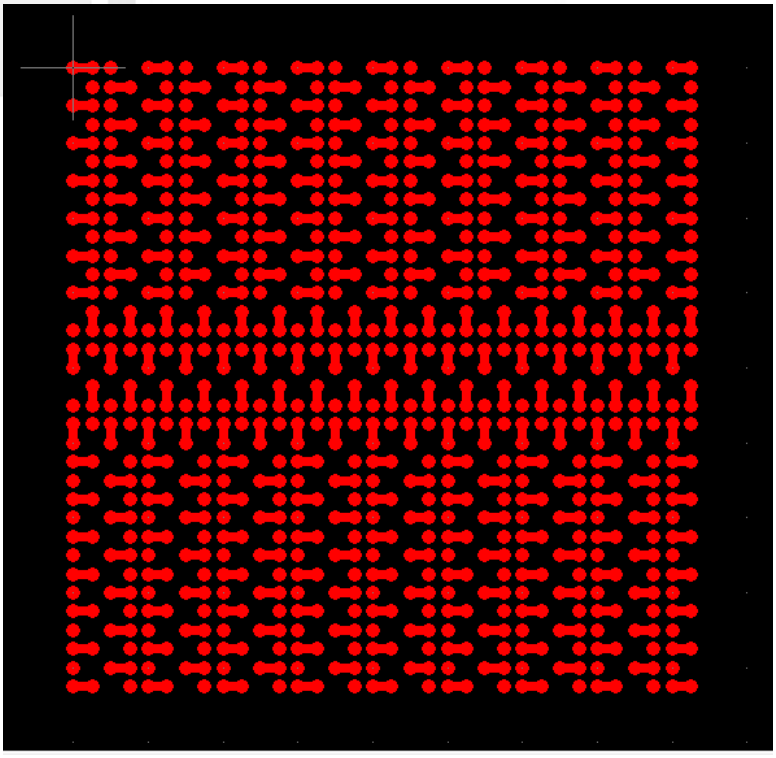


In the following section we show the individual layers and route patterns.

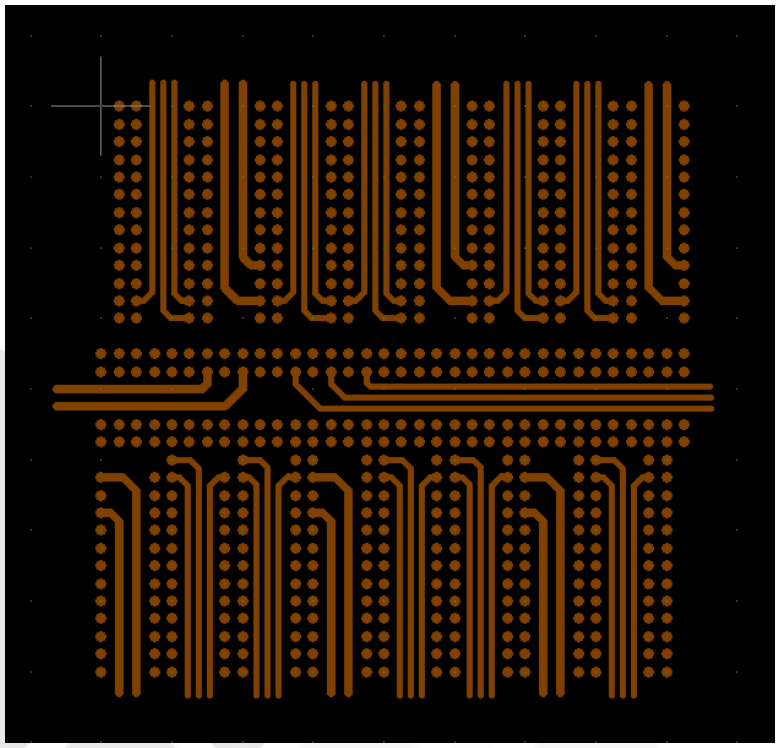
Outer layer image, the microvias are drilled directly into the BGA pad.



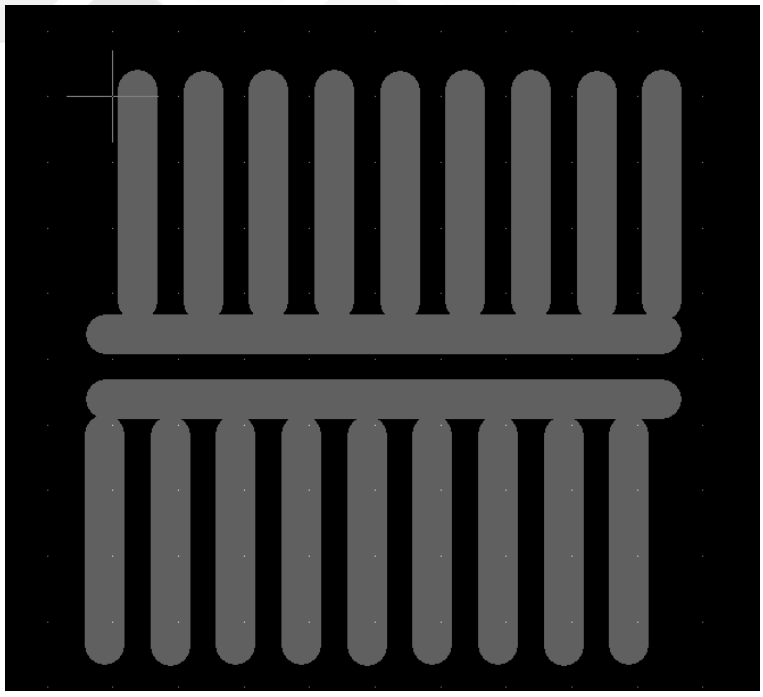
First internal layer (L2) with landing pads for the microvias and the redistribution to the VeCS slot.



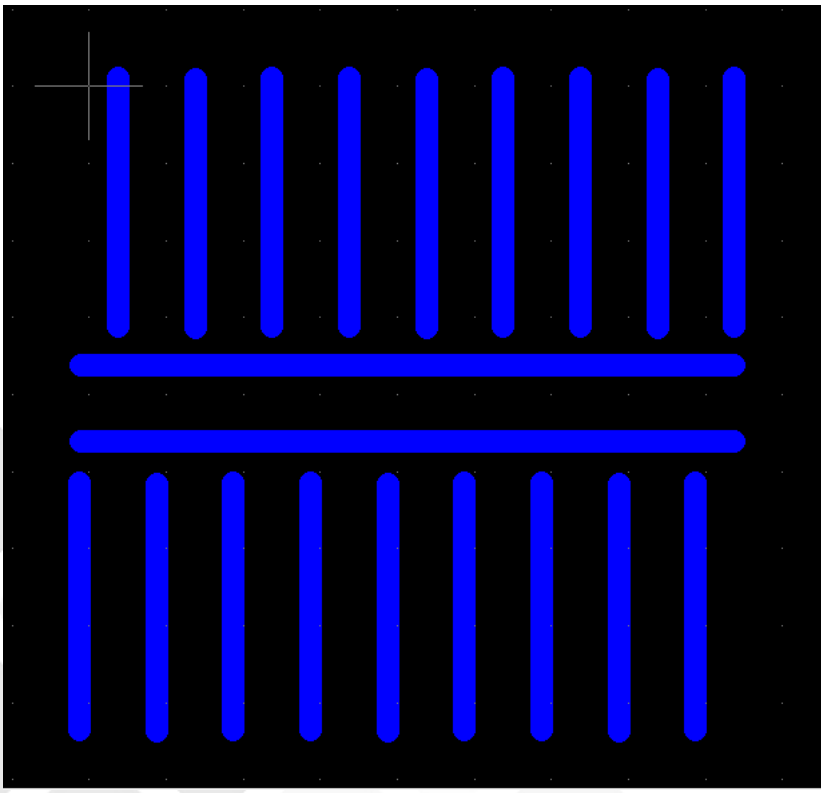
Signal layer showing several different line widths and spacing. As shown we can run 2 traces of 0,12mm and 0,12mm gaps or a 3 traces of 0,08mm and 0,08mm gap.



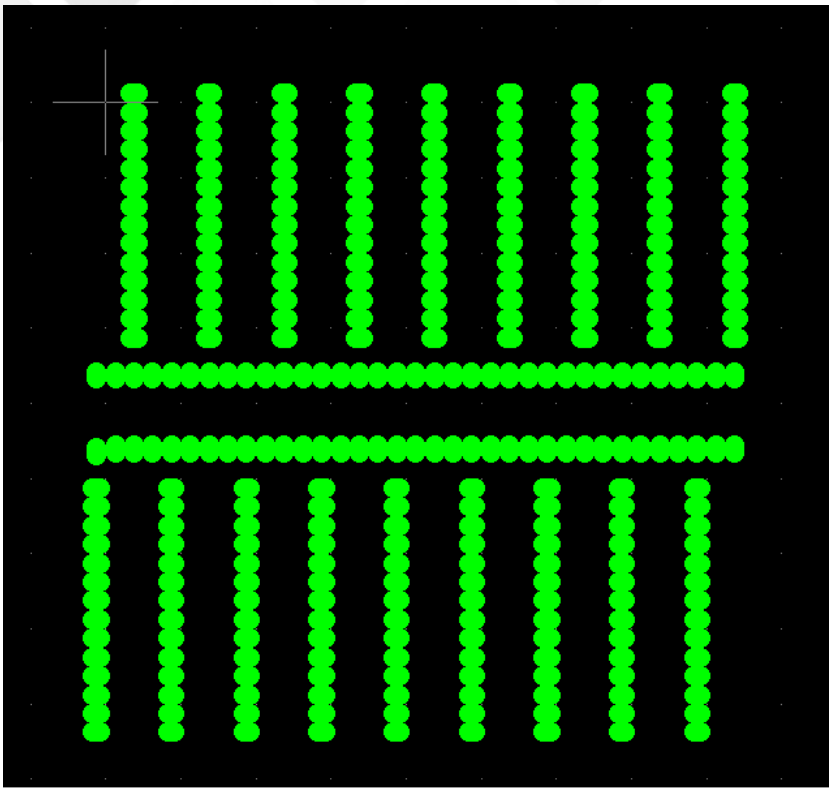
The ground or power layer is shown below in reverse. No connection to the VeCS are shown. These can be added by adding a trace. The slot to plane spacing used here is 0,15mm.



In the following images we show the slots and second route images.



Second drill data.



This application note is generic and can be adjusted to your specific needs. If you have an application / a package and pin assignment we will provide you a set-up recommendation for VeCS and stack-up.

Please contact us on info@nextgin-tech.com.