Vertical Conductive Structures—a New Dimension in High-Density Printed Circuit Interconnect

by Pete Starkey
I-CONNECT007

From our previous conversations, I knew that Joan Tourné was working on a novel high-density interconnection concept. Having eagerly awaited the chance to discuss the technology in detail, I was delighted when he contacted me to confirm that his IP had been secured and that he could now talk openly about VeCS, the Vertical Conductive Structure designed to provide a cost-effective alternative for complex fan-out from fine-pitch grid array components.

Knowing Tourné's long-term background in high-end PCB technology, from his many years as technical director at Mommers Print Service in the Netherlands, and subsequently as advanced technology and business director with Viasystems, I was curious to learn about his latest enterprise.

***Starkey:** Joan, it's great to speak with you again. Tell me a little about NextGIn Technology BV.*

Tourné: Yes, Pete, good to see you. NextGIn is a fabless shop based in the Netherlands, with extensive experience in the design and manufacture of high-end circuitry and a "make it happen" mentality. We are developing interconnect solutions for our partners in the semiconductor packaging and printed circuit board industries who need to advance their product performance or to cost-reduce their product. Presently we are working with a small group of selected OEMs in datacom, telecom and data processing markets to design and test our VeCS technology.

***Starkey:** What was the rationale behind the development of VeCS and what is the need for an alternative PCB concept?*

Tourné: The big limitation of established HDI technologies is the density of vertical interconnections that can be achieved without going through many stages of sequential build-up. Grid array packages are driving PCB complexity, and PCB manufacturing technology is lagging. Through-hole techniques take up too much space, and we have got to the stage where holes cannot be placed closer together. Sequential build-ups are an expensive solution, and as the build-up construction gets more complex, the yield goes down. The challenge of routing

conductors under fine-pitch grid arrays becomes increasingly difficult and is effectively a constraint on package development. And power distribution into the core of the package becomes difficult and expensive.


Joan Tourné

***Starkey:** So how does your "vertical conductive structures" concept overcome these limitations?*

Tourné: Not only can we achieve higher interconnection density by packing more vertical connections in a smaller space, at the same time we can increase conductor routing channel density under grid array components. And we can do this without reducing line widths or spacings, so we can maintain high transmission line speed and enhance signal integrity by better signal-to-plane reference and higher current-carrying capacity in and out of the grid array. And because we don't need to use sequential build-up technology, we reduce cost.

***Starkey:** That sounds very impressive. What are the key characteristics?*

Tourné: VeCS is based on special formed cavities that can connect to multiple internal layers using less space than vias or microvias, leaving more room for conductor routing under area array components like BGAs. For example, a 0.65 mm pitch BGA can be successfully routed with VeCS, whereas a fan-out would not be possible with traditional vias. And VeCS causes much less disruption to ground and power planes and reference layers, which with traditional via technology would be reduced to a few small slivers of copper under the BGA. At the moment, we have test vehicles in manufacturing with a 0.4 mm pitch using single lamination processes.

***Starkey:** From the PCB fabricator's point of view, does VeCS technology require substantial capital investment or significantly different process chemistry?*

Tourné: No, to both parts of the question. No direct new capital equipment is required, and the technology is well within the established capability of any high-end board shop after appropriate training and licensing.

***Starkey:** So how do you form these cavities?*

Tourné: There are several options, but let me describe a very basic example: Drill a row of holes, in the diameter range 0.1 mm to 0.5 mm, close together and separated by narrow webs of material. Remove these webs of material by drilling, routing or laser cutting, preferably on the same machine to achieve best registration. Once the structure has been formed, use standard PCB processes to clean, metallise and plate-up, then image and etch the surface conductor pattern. Finally, selectively remove copper from the plated cavity by drilling, to leave vertical copper traces where conductors are required. Perhaps a schematic diagram would help you to visualise the result (Figure 1).

***Starkey:** So how does this compare with conventional through-hole interconnection?*

Tourné: The hole is replaced by a vertical trace or half-cylinder. The vertical trace is preferred for signal integrity performance. The structure can be filled and overplated depending on the application. More vertical connections can be created for a given surface area and, for imped-

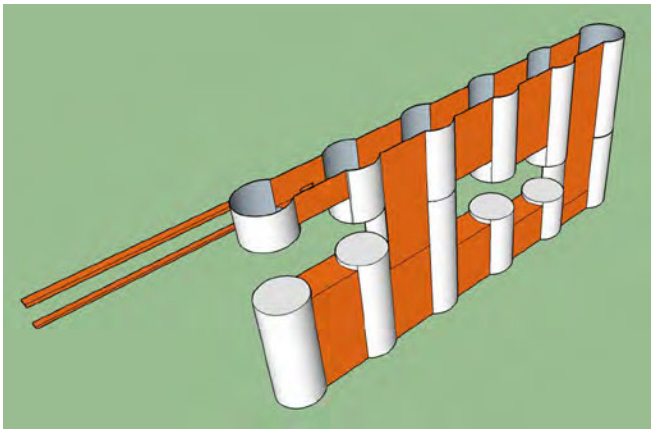


Figure 1: Schematic diagram of VeCS.

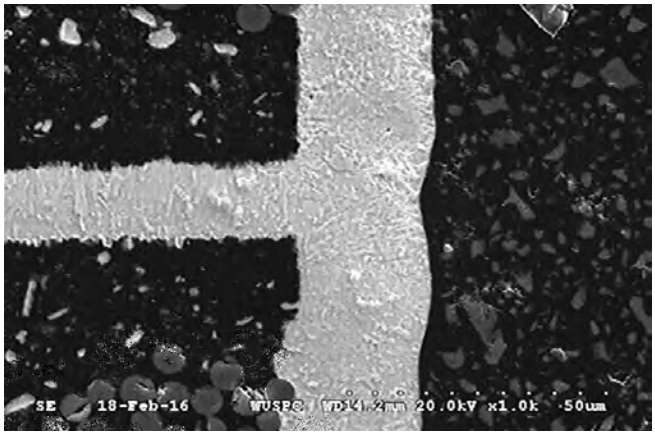


Figure 2: Cross-section of the interconnect with the innerlayer.

ance control, signal and ground conductors can be designed to face each other across the cavity. Another benefit is that there is no CAF path between vertical traces.

***Starkey:** You mentioned cost savings. How do costs compare with conventional constructions and where are the savings made?*

Tourné: The cost reduction is realised by making more efficient use of the conductor routing space and therefore reducing the layer count of the board. We offer design analysis service to demonstrate how VeCS can reduce cost in your product. With the use of more expensive materials, the reduction in the BOM cost is becoming significant. In various analyses conducted last year, we have demonstrated cost reductions in the range of 15% to 40%. In future articles, we can present cases of the cost reduction analysis.

***Starkey:** How far down the road are you with VeCS technology?*

Tourné: We've progressed a long way since demonstrating the initial proof of concept, and we continue to work closely with leading OEMs and fabricators. One manufacturing example is a 12-layer test board, 2.2 mm thick, on MEGTRON6, with 0.5 mm, 0.75 mm, 0.8 mm and 1.0 mm BGAs routed on the same panel. We have subjected samples of this construction to six reflow cycles at 288°C, and found no evidence of interconnection failure. Results after six solder shocks at 288°C were similar (Figure 2). And we have taken daisy-chain test panels through multiple reflow cycles followed by thermal cycling to failure, with results comparable with through-hole examples. Regarding impedance control and signal integrity, I can show you some remarkably good TDR traces from the area under the BGA.

***Starkey:** What about design? Do any of the major CAD vendors offer the capability to generate designs based on VeCS technology?*

Tourné: At the moment, we have two CAD software houses working on the technology and they have demonstrated capability already.

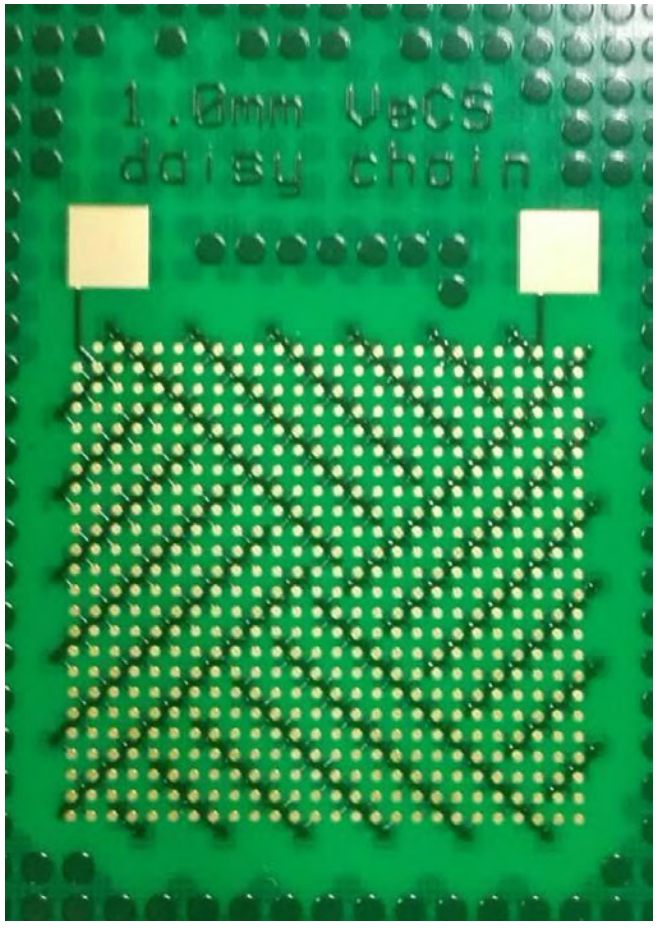


Figure 3: Board with daisy chain on 1.0 mm pitch using VeCS technology used for reliability testing of the interconnects. The fabrication and testing is done by WUS.

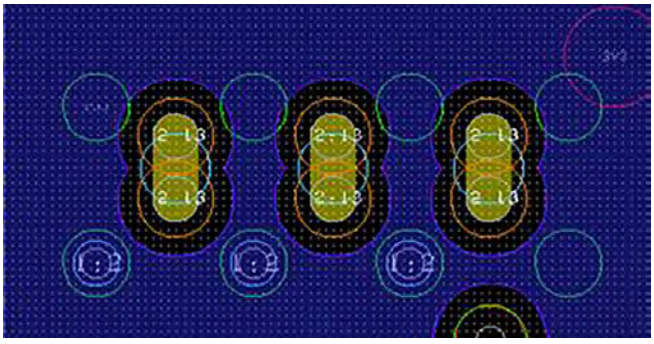


Figure 4: VeCS technology in Altium design system.

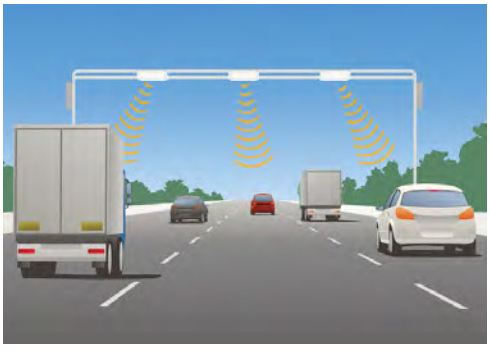
They have seen the advantage of the technology and continue exploring VeCS technology. We have also developed workarounds in some of the CAD systems, as shown in Figure 4. There is still some manual work, but we can demonstrate the technology and gain advantage of the VeCS benefits. We can also train and qualify your preferred PCB suppliers, and offer training to the OEM under a license agreement.

***Starkey:** Joan, I am very grateful for your time in introducing me to what I could confidently describe as a potentially disruptive PCB technology.*

Tourné: Thanks for your interest, Pete. But I have only given you a glimpse of what this technology has to offer. I hope you have gained an understanding of the fundamental principles of what we can achieve. There is so much more I could explain about practical aspects, application opportunities and the VeCS technology roadmap. I would be delighted to prepare a series of detailed articles if you believe they would appeal to the designers and fabricators among your readers.

***Starkey:** That's a splendid offer, Joan, and well worth pursuing. Many thanks, again.* **PCB**

Telematics to Shape Cockpit and Cabin Strategies



One in four passenger vehicles sold by 2025 is poised to feature digital instrument clusters, dedicated passenger infotainment systems, and integrated biometrics with bought-in device functionality. Original equipment manufacturers (OEMs) are grappling to design components that are in line with fast-changing technology trends and customer expectations.

"The luxury segment car of the future will have augmented reality HUD, OLED displays, interactive cabin doors and windows, advanced biometrics, and ample infotainment for passengers," said Frost & Sullivan Intelligent Mobility Research Analyst Joe Praveen Vijayakumar. "The mass-market car segment cockpit will have temperature-controlled seats, Combiner HUD, TFT LCD displays and substantial biometrics features for vehicle security, Driver Monitoring and Health Wellness and Wellbeing (HWW)."

Cockpit and Cabin Strategies of Automakers, 2016–2025 is part of Frost & Sullivan's Mobility: Automotive & Transportation Growth Partnership Service program. According to the research, advancements in technology will influence every component of the cockpit, ushering in an era of new travel experience, dedicated instrument clusters and infotainment screens.

Leading players have adopted various strategies to gain market share and competitive advantage, including a light-diffusing fiber, which is an alternative to separately weaving light-emitting diode into interior fabrics for ambient lighting, developed by Corning; a solar-powered, organic, light-emitting-diode-fitted transparent car roof in partnership with BASF, in development by Philips.

"Biometrics will be an integral part of cockpits and cabins of the future, and OEMs and suppliers should pursue partnerships with innovative biometric companies or fund relevant nascent start-ups," noted Praveen.